LARGE SCALE INTEGRATION -

A DESIGNER'S VIEWPOINT

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The research in this paper was supported in part by the National Science Foundation (GJ 32758x). This document has been approved for public release and sale; its distribution is unlimited.

ACKNOWLEDGEMENT

Acknowledgement and appreciation is due to Mrs. Dorothy Josephson for typing the final manuscript and to Mercedes Kostkas for formatting and layout. Also, we acknowledge all those responsible for the existence and maintenance of the CMU-LDX System on which this document was produced.

ABSTRACT

Large Scale Integration (LSI) has conjured up such exciting possibilities as a computer-on-a-chip among both users and suppliers in the last five years. There have been many diversified efforts. This has resulted in a large non-trivial array of device technologies, manufacturing methods, interconnection methods and packaging schemes. In fact at a recent solid state conference after hearing words like RTL, ECL, PMOS, CMOS, MNOS, etc. an engineer was overheard crying out "SOS" and it was interpreted as a comment on a new technology (silicon on sapphire). With this state of affairs in mind we felt that a comprehensive report surveying the LSI field, had to be prepared in order to guide research on computer structures. Therefore this report surveys the existing state of the art in LSI along different dimensions. The topics include:

1. the circuit technology (RTL, DTL, TTL, etc.);

2. the manufacturing techniques for bipolar devices (collector Diffused Isolation, Isoplanar techniques, etc.) and MOS devices (PMOS, Si-gate, Moly-gate, etc.);

3. interconnection schemes for customizing circuits (discretionary wiring, micromatrix, polycell, etc.);

4. packaging techniques from the viewpoint of hermiticity, pin count, reliability, etc.;

5. logic functions, especially Semiconductor memory arrays which form a very important application of LSI, are discussed together with some forecasting on price and volume;

6. the implication of LSI on large modular system design,

It is hoped that a reading of this paper by people having a basic knowledge in Electronics and Integrated Circuits would give enough background in the state of art in LSI to be able to choose certain device technology, fabrication method and packaging techniques for their applications. It should also give the reader an ability to understand the contemporary literature in LSI and the directions the industry will take over the next five years.

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I. LSI TECHNOLOGY

The invention of solid state devices like the transistor and diodes brought about a new era in the electronic industry. The size of the electronic component was drastically reduced and the reliability increased by an order of magnitude. The next major step was the development of silicon planar technology which reduced the size of the device to a few square mils. This formed the beginning of integrated circuits. Efforts were made to produce silicon chips* as large as possible and to grow devices on it so that the area (real estate) used by each device was as small as possible. As the ability to reliably manufacture circuits increased, various degrees of integration marked the generations: Small Scale Integration (SSI), Medium Scale Integration (MSI) and Large Scale Integration (LSI). The degree of integration depended on the density of interconnected devices and the area of the chip.

A. WHAT IS LSI

Wickes (1969) in his paper discriminates between SSI, MSI and LSI by the number of logic gates implemented on each chip. A single equivalent logic gate is taken as the fundamental building block. On this basis an SSI circuit is one which has 1~12 equivalent logic gates, an MSI circuit is one which has 12~100 logic gates and LSI circuit is one which has more than 100 logic gates. (E.g., currently produced random access bipolar memory modules have approximately 500 equivalent gates and other advanced modules are expected to have four times the number.) With the success of LSI, there will come Extra Large Scale Integration (ELSI), Ultra large Scale Integration (ULSI), etc.

From the discussion above it seems clear that a Large Scale Integrated circuit chip would have the ability to perform a very complex logic function, or a large number of simple logic functions.

B. THE SPACE OF LSI DEVICES AND PROCESSES

The process for producing LSI chips is a direct evolution of the process initially used to fabricate the single solid state device. The process consists of several major steps such as preparation of the silicon wafers, epitaxial growth, oxide growth, impurity diffusion and oxide etching. It is not intended to describe the process here, as these are given in various texts (Khambata 1969). Instead we wish to look at the different devices and processes that were developed over the years to meet user needs. This, we believe, would give some structure to the array of devices and processes which otherwise seem to have developed in a haphazard manner. Figure 1 gives the way in which we intend to divide discussion on LSI technology. As can be seen from the diagram there are a number of dimensions. The development in these different dimensions has been directed towards satisfying different user needs. For this reason the space of user needs is first described.

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*A chip is a tiny piece of semiconductor material, broken from a monolithic semiconductor wafer, on which one or more electronic components are formed.

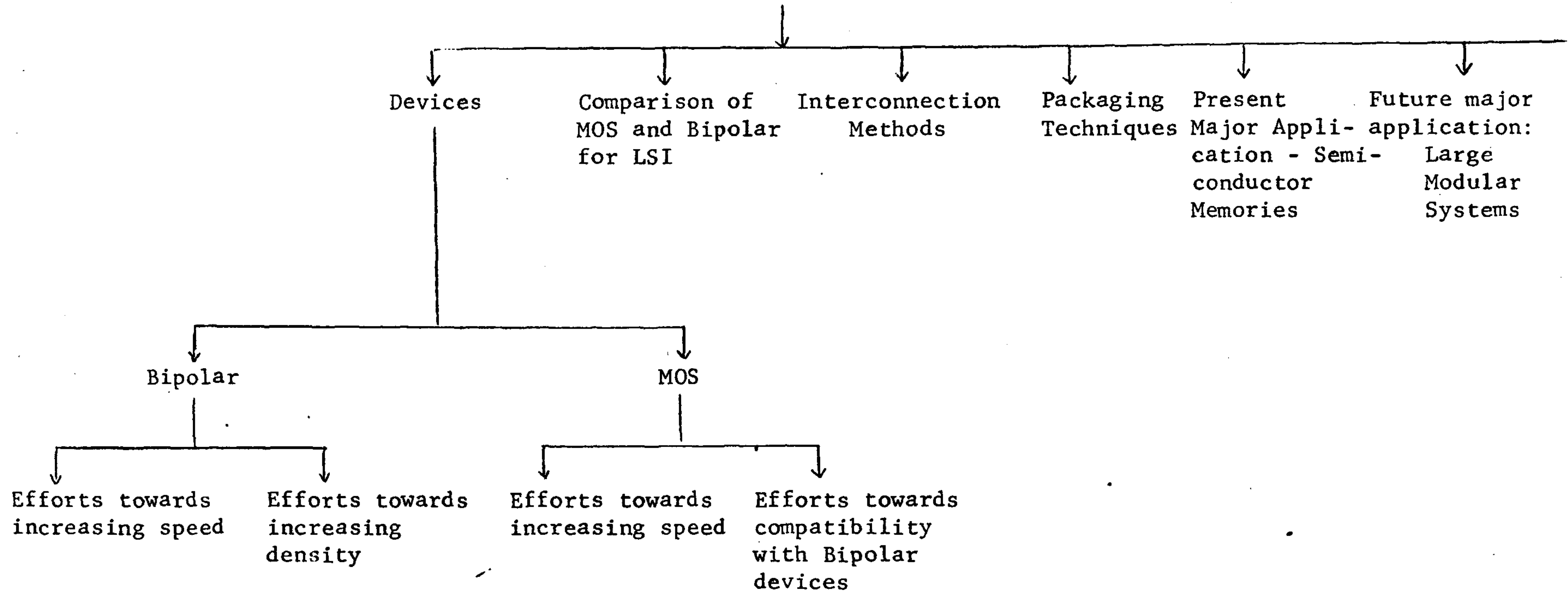

Fig. 1. Aspects of LSI Technology

The important dimensions of this space for digital LSI circuits can be easily enumerated: The speed of the circuit, the size of a single device, the cost/device, the power dissipation/device, the reliability of the circuit, the ease of handling of the circuit elements, and the compatibility of the circuits with the existing elements. Each of the above user requirements in some sense allowed the industry to develop new devices and processing techniques to gain additional markets.

II. LSI DEVICES

There are two basically different types of devices that are manufactured for LSI circuits: Bipolar and Metal Oxide Semiconductor (MOS) devices. In the following sections we will examine each device type in more detail.

A. BIPOLAR DEVICES

Bipolar devices preceded MOS devices and hence have the advantage of experience and familiarity. There were two main efforts. One was in increasing the density of devices by using different fabrication techniques and the second was in increasing the speed by using different circuit configurations.

1. Efforts towards increasing density.

Bipolar devices consume a considerable amount of chip area in isolation between neighboring devices.Isolation between different devices is required as more than one device is fabricated on the same chip.Therefore the efforts towards increasing density were directed at reducing the area of the isolation region between two devices.The processes that evolved to improve on the Standard Buried Collector process for fabrication of Bipolar devices were:

(1) collector diffused isolation,

(2) base diffused isolation,

(3) isoplanar process.

The above processes together with the Standard Buried Collector process will be described briefly.

a. Standard Buried Collector Process

The standard buried collector process starts with a P-type substrate on which an N-type layer is epitaxially grown (see Figure 2a to Figure 2d). On top of this N-type epi layer SiO_2 is grown. (This SiO_2 performs two important functions. It behaves as a passivating layer for any external impurities and it also can be used as a mask for selectively depositing the active components into the N-layer beneath.) This SiO_2 is then selectively etched from the places where isolation diffusion has to be performed. This wafer is then subjected to a P-type diffusion process. This leaves isolated N-type regions surrounded by deep P-type diffused regions. The n-type regions then, are used as collector for an NPN transistor. Then a thin film of SiO_2 is regrown over the exposed regions. The process of etching of SiO_2 is repeated, but this time it is removed at places where a base is to be diffused. A shallow P-type diffusion is then performed which forms the base of the transistor. The cycle of SiO_2 growth, oxide etching and an N diffusion is again repeated to give the emitters of the transistors. During the emitter diffusion some SiO_2 film over the n-type collector region is also

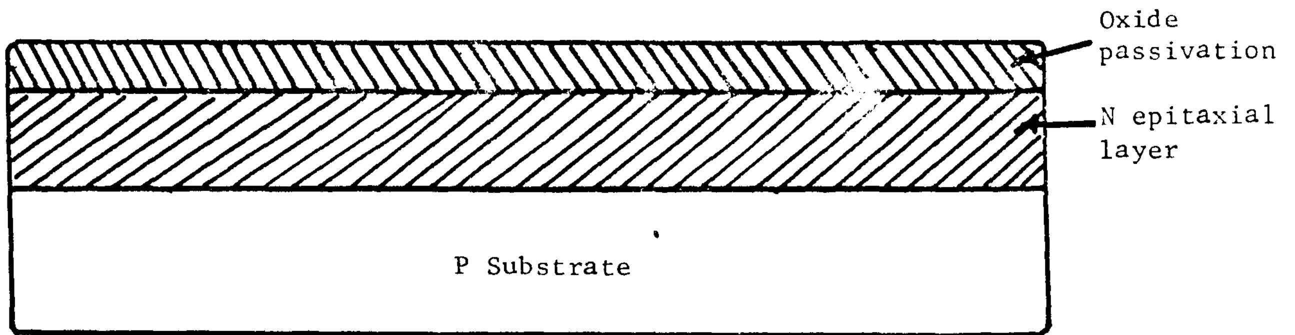

Fig. 2(a) Original Substrate.

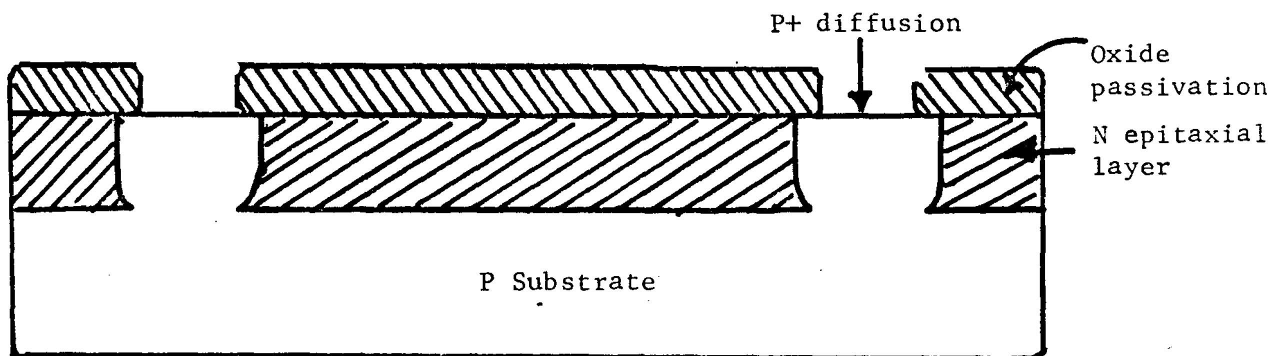

Fig. 2(b) First Diffusion for Isolation.

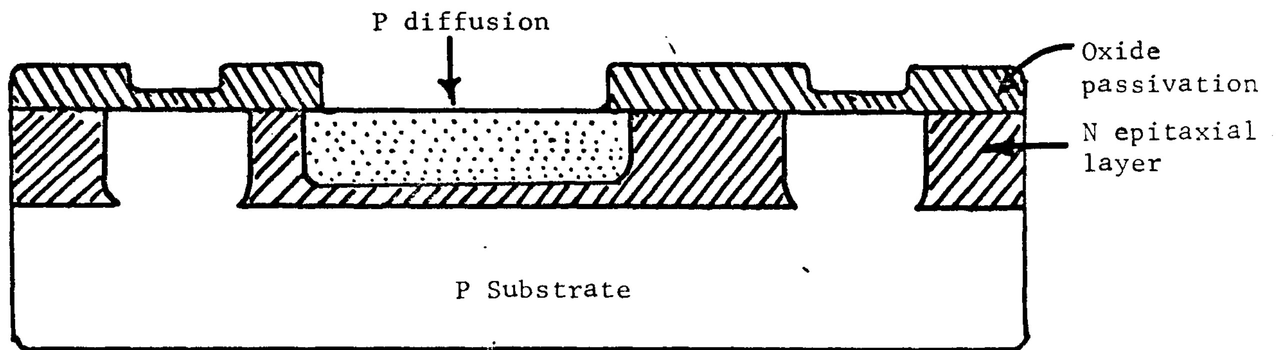

Fig. 2(c) Second Diffusion for Transistor Base.

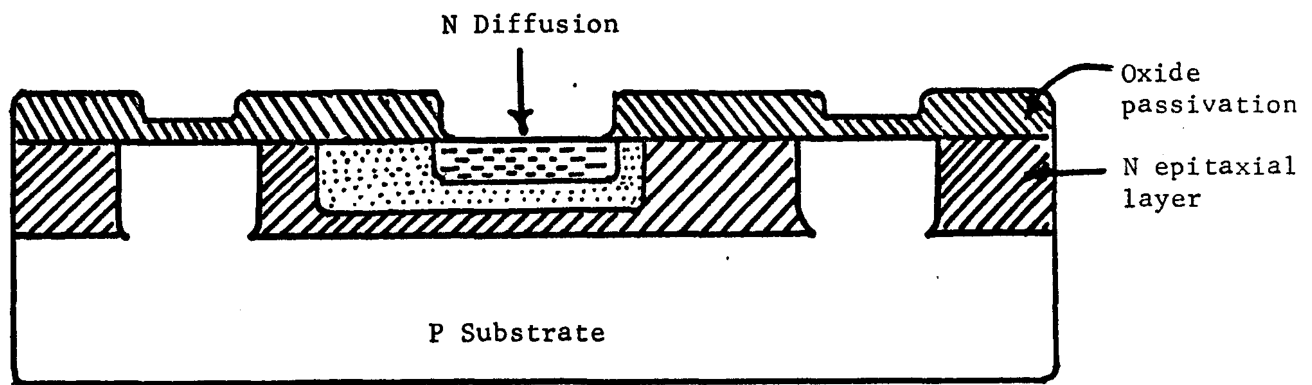

Fig. 2(d) Third Diffusion for Transistor Emitter.

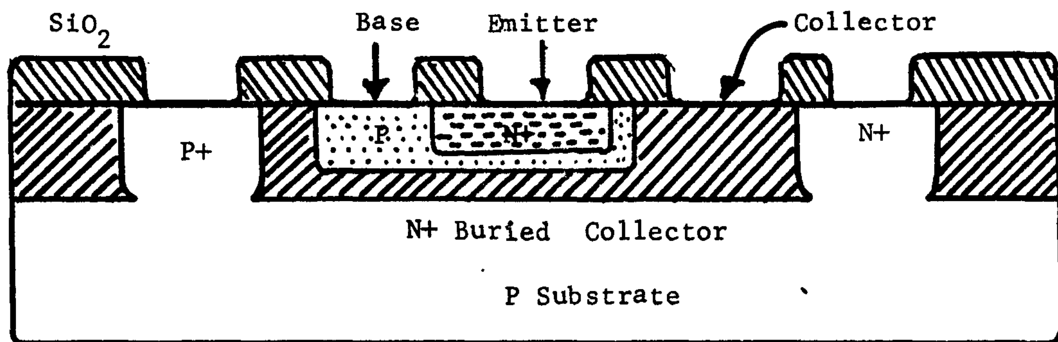

Fig. 2(e). A Standard Buried Collector Transistor.

Fig. 2. Fabrication Steps in a Standard Buried Collector Transistor.

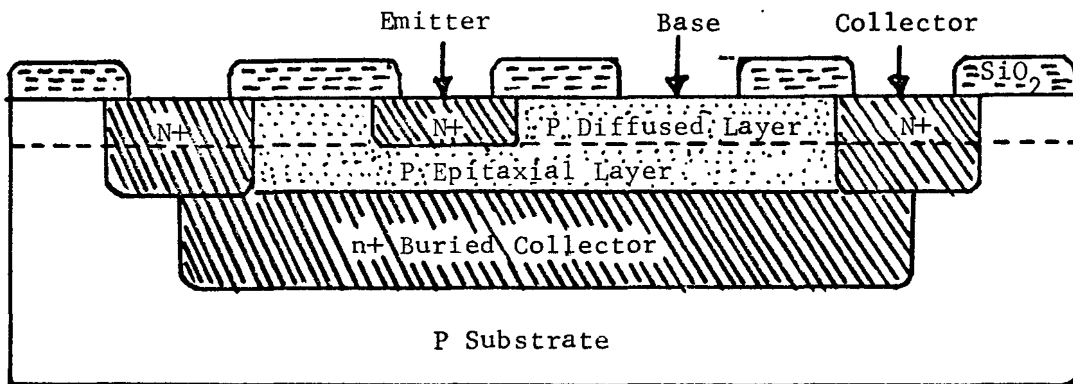

Fig. 3. Structure of Collector Diffused Isolated Transistor.

removed to diffuse some n-type impurities for collector contact area. This is necessary as aluminium, a p-type material, is used for contact and would form a p-n junction with the collector rather than a good ohmic contact. Finally again SiO_2 is grown and etched at places where the aluminium interconnecting pattern is to be formed. Aluminium is evaporated over the whole surface and due to its properties it clings to both SiO_2 and the exposed component contacts. The unwanted aluminium is then etched off.

As can be seen from the above process the fabrication consists of a few different repetitive steps. The process is rightfully named Buried Collector as collector region is the deepest region of the transistor.

b. Collector Diffused Isolation

In a standard buried collector structure shown in Figure 2e it can be seen that a p+ isolation diffusion is used between the transistors. This diffusion increases the total area required per transistor and also requires some extra fabrication steps. The Collector Diffused Isolation (CDI) scheme (Murphy et al., 1969) overcomes this difficulty. Figure 3 shows a cross section of a CDI device.

In the CDI process the first two steps are the same as in the standard process. A p-type substrate is taken in which a n+ buried layer is diffused. A p-type layer is then grown epitaxially on the substrate. An n-type collector is then diffused selectively into this epitaxial layer to make contact with the n-type buried layer at its periphery. A p-type base diffusion is performed which improves the properties of the transistor. Finally the emitter is diffused, holes are made in the oxide and aluminium is used for the contacts.

The N-type collector is always operated at a positive voltage with respect to p-type substrate to bring about the required isolation. This technique achieves a higher density and higher yield as the device is smaller and the number of fabrication steps are less than in the standard buried collector case. Consequently the manufacturing cost is cheaper.

c. Base Diffused Isolation

This technique discussed by Defalco (1971) is essentially useful for low power circuits. To fabricate this device a p substrate is used on which a shallow n epitaxial layer is grown. (See Figure 4.) For low power circuits a buried n+ collector is not required as the currents are small. Then a p+ diffusion is made to get a base and its surrounding base isolation. Then the emitter and collector diffusion together with the required contacts are made as normal.

The isolation, in this technique, is accomplished by applying a negative voltage to the base-isolation region. The negative voltage brings about a depletion region which punches through the shallow epitaxial layer into the p-substrate. (The dotted lines indicate the extent of depletion region in the n layer.) The disadvantage of this circuit is that it requires an extra power supply. But the current required is quite low and the supply with its distribution network does not have stringent requirements.

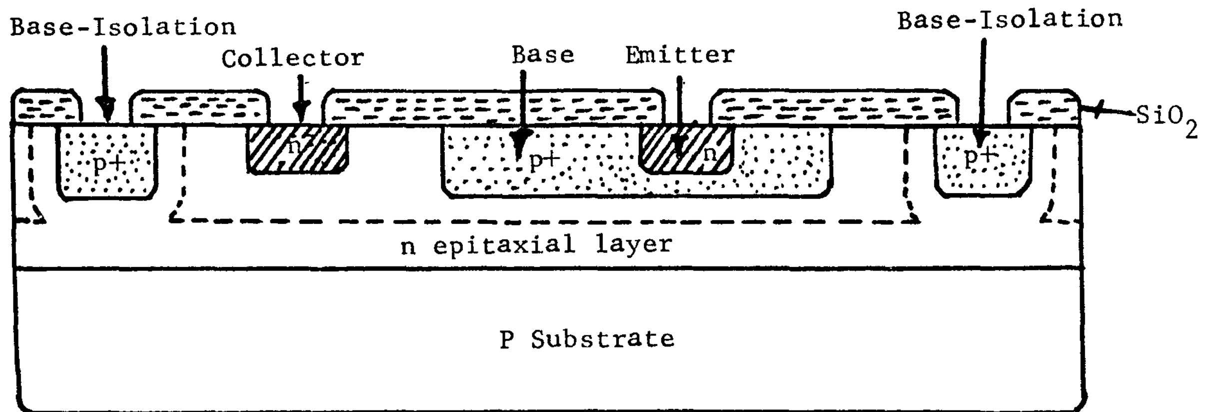

Fig. 4. Structure of Base Diffused Isolation Transistor.

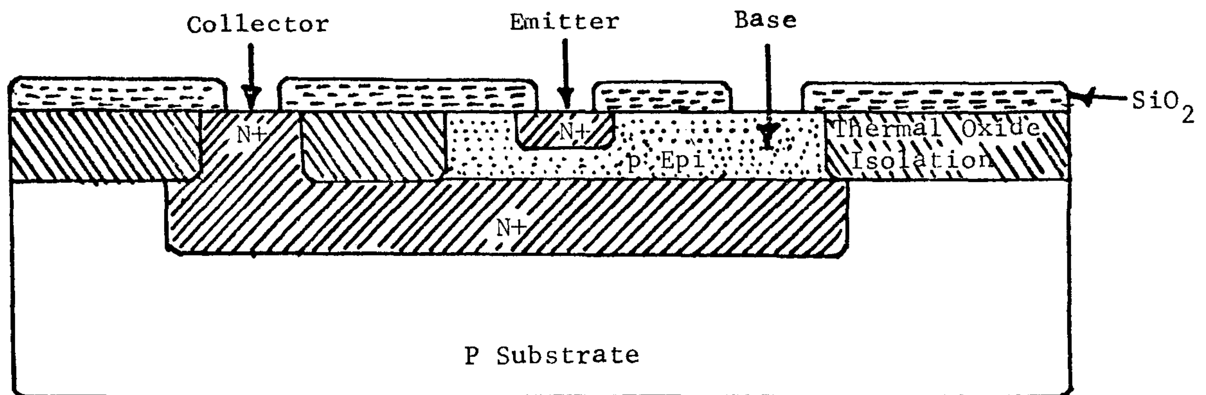

Fig. 5. Structure of an Isoplanar Transistor.

d. Isoplanar Technique

This technique discussed by Defalco (1971) brings about a reduction in area for a device by using a special property of Silicon Nitride (Si_3N_4). Si_3N_4 is used as a protective layer on silicon during the fabrication to prevent oxidization. Thus better alignment is possible. This process also uses Silicon Dioxide (SiO_2) for isolation between devices.

The process begins, as usual, with a p-substrate (see Figure 5). An N+ buried layer is diffused and a shallow N epi layer grown on the substrate. Next Si_3N_4 is deposited on top of the whole chip and selectivelly etched wherever oxide isolation is to be accomplished. SiO_2 is thermally grown in these etched areas. This SiO_2 surrounds the base and collector regions. Then, as seen in Figure 5, a p+ diffusion for base and n+ diffusion for collector and emitter are performed.

The result of this process is that the collector contact diffusion and base diffusion are completely surrounded by SiO_2, thus isolating the device. The SiO_2 and Si_3N_4 bring about self alignment thus improving the device characteristics. It is projected that this process, which was developed by Fairchild, would produce a device approximately half the size of the CDI process. Fairchild has already produced a 256 bit Random Access Memory (RAM) with the following specifications:

chip access time - 20 nsec
read access time - 50 nsec
circuit - TTL
power dissipation - 2mw/bit
chip size 96 mil x 126 mil

They also have a 1024 bit RAM in development (circa mid 1971). Since the structure of the device is co-planar it essentially has higher reliability and yield.

Finally note that the efforts towards increasing device densities on a chip for bipolar devices have been quite successful, It would not be an impossible goal to reach the device densities of current MOS processes. Table 1 gives a comparison of the complexity of the processes described so far. It can be seen that the BDI process should be the cheapest to handle as the number of masks, which forms the major cost of an LSI device, is smallest (see Table 1). But BDI is useful for low power only. Isoplanar, having very high densities, requires nearly the same number of steps as the standard Buried Collector (SBC) structure and seems to be the most promising.

2. Efforts towards increasing speed

In Bipolar devices the speed improvement in Logic Circuits was accomplished by the use of different coupling elements between the transistors. Initially the basic discrete component logic circuits, like the Resistor Transistor Logic (RTL), were

	Standard Buried Collector	Collector Diffused Isolation	Base Diffused Isolation	Isoplanar
Mask	6	5	4	6
Oxidations	4	3	2	4
Diffusions	4	3	2	3
Epitaxial Layer	1	1	1	1

Table 1. Comparison of processing steps in fabrication of Bipolar Devices by various methods [Defalco (1971)].

Parameters	RTL	Low Power RTL	DTL	12-ns TTL	6-ns TTL	4-ns ECL	2-ns ECL	1-ns ECL	P-MOS	C-MOS
1. Circuit form	←resistor-transistor→		diode-transistor	←transistor-transistor→		←emitter-coupled current mode→			p-channel MOS	complementary MOS
2. Positive logic function of basic gate	← NOR →		← NAND →			← OR/NOR →			NAND	NOR or NAND
3. Wired positive logic function	←implied AND (some functions) →		implied AND (A-O-1)	← AND-OR-INVERT →		← implied OR (all functions) →			← none →	
4. Typical high-level Z_0 ohms	640	3.6 k	6 k or 2 k	70	10	15	6	6	2 k	1.5 k
5. Typical low-level Z_0	R_{sat}	R_{sat}	R_{sat}	R_{sat}	R_{sat}	15 ohms or 2.7 mA	6 ohms or 6.7 mA	6 ohms or 21 mA	25 k	1.5 k
6. Fanout	5	4	8	10	10	25	25 inputs or 50 ohms	10 low-Z inputs or 50 ohms	20	50 or higher
7. Specified temperature range, °C	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75	-55 to 125 0 to 70	-55 to 125 0 to 75	-55 to 125 0 to 75	-55 to 125 0 to 75	0 to 75	-55 to 125 0 to 75	-55 to 125
8. Supply voltage	3.0V±10% 3.6V±10%	3.0V±10% 3.6V±10%	5.0V±10%	5.0V±10% 5.0V±5%	5.0V±10% 5.0V±5%	-5.2V+20% -10%	-5.2+20% -10%	-5.2V±10%	-27±2V -13±1V	4.5 to 16V
9. Typical power dissipation per gate	12 mW	2.5 mW	8 mW or 12 mW	12 mW	22 mW	40 mW	55 mW plus load	55 mW plus load	0.2 to 10 mW	0.01 mW static ≈ 1mW at 1 MHz
10. Immunity to external noise	nominal	fair	good	very good	very good	good	good	good	nominal	very good
11. Noise generation	medium	low-medium	medium	medium-high	high	low	low-medium	medium	medium	low-medium
12. Propagation delay per gate, ns	12	27	30	12	6	4	2	1	300	70
13. Typical clock rate for flip-flops, MHz	8	2.5	12 to 30	15 to 30	30 to 60	60 to 120	200	400	2	5

Table 2. - continued on next page

Parameters	RTL	Low Power RTL	DTL	12-ns TTL	6-ns TTL	4-ns ECL	2-ns ECL	1-ns ECL	P-MOS	C-MOS
14. Number of functions; family growth rate	high; growing	high; growing	fairly high; new functions in TTL	very high; growing	very high; growing	high; growing	high; growing	high; growing	low; growing	low; growing
15. Cost per function	low	low	low	low	medium	low	medium	high	medium to high	medium to high

Table 2. Comparison Chart of the Major IC Digital Logic Families (adopted from Garret 1970)

directly mapped into Integrated Circuits (IC's). RTL was slow and had inherent problems.* Thus, other circuits like Diode Transistor Logic (DTL), Transistor Transistor Logic (TTL) and Emitter Coupled Logic (ECL) were devised. Each one of these circuits has a particular advantage and were listed roughly in order of increasing speed. Figure 6 gives some of the typical logic circuits. Table 2, taken from Garrett (1970), gives typical propagation delay times and other characteristics for circuits of different technologies. Schottky TTL (circa 1970) was introduced to compete with ECL for speed. Note that manufactureres like Texas Instrument developed high speed TTL in an attempt to satisfy the speed requirements, and Low Power TTL in an attempt to satisfy power requirements for TTL users. TTL, High Speed TTL and Low Power TTL circuits have compatible voltage swings. Therefore a designer could mix them in a circuit to achieve optimum performance. Of the different logic circuits described, at low level of integration, TTL and ECL are currently the most popular with logic circuit designers.

B. METAL OXIDE SEMICONDUCTOR DEVICES

Metal Oxide Semiconductor (MOS) technology is more recent and has not yet reached the high state of development of bipolar technology. Therefore, in comparison with Bipolar technology, there are many more choices for a designer as the manufacturers have not yet settled on a particular circuit type, fabrication technique, etc. Some of the ways for classifying MOS are:

(1) the type of circuit p channel (p-MOS), n-channel (n-MOS) or Complementary MOS (CMOS)

(2) the type of gate conductor (Al gate, Si gate or Molybdenum gate)

(3) the type of insulator used (Silicon Dioxide, Silicon Nitride or Aluminium Oxide)

(4) Crystal Orientation (111 as against 100 orientation) and

(5) the substrate used (p-substrate, n-substrate or Silicon on Sapphire).

MOS devices inherently consume a smaller area when fabricated (due to its self isolation property) and have a simpler process of fabrication. Hence the main efforts in MOS devices have been to increase the speed of the devices and to make them compatible with existing Bipolar circuits. The latter can be achieved by reducing the threshold voltage of a MOS device.

The threshold voltage of a MOS device is defined as the minimum gate voltage required to invert the surface of the Silicon underneath the gate electrode to the point where the channel just becomes conductive. An equation (Wilder, 1970) for the threshold voltage can be given as

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*It is difficult to fabricate a resistor using IC technology, because of stringent tolerance limits. Resistors also require a large chip area.

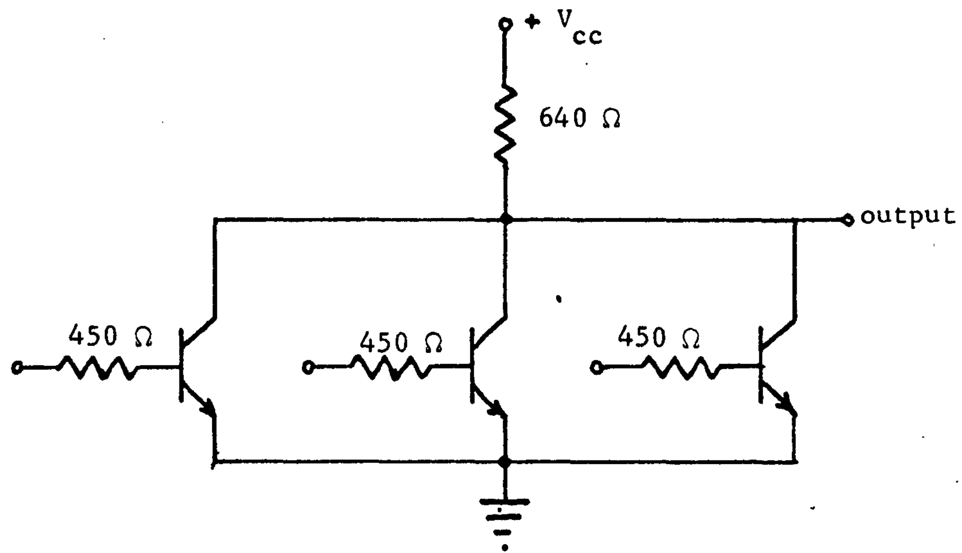


Fig. 6 (a)
A Standard RTL Gate

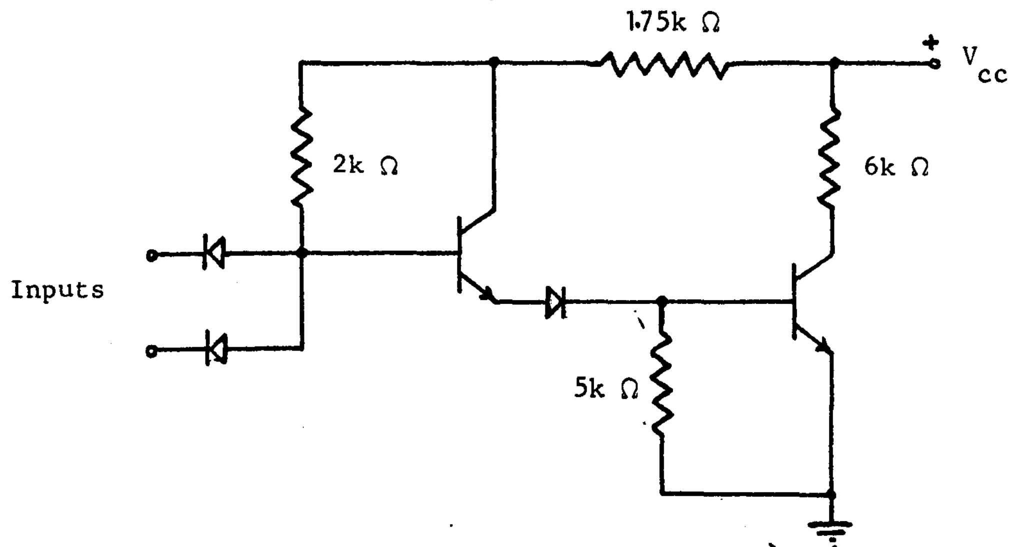


Fig. 6 (b)
A Standard DTL Gate

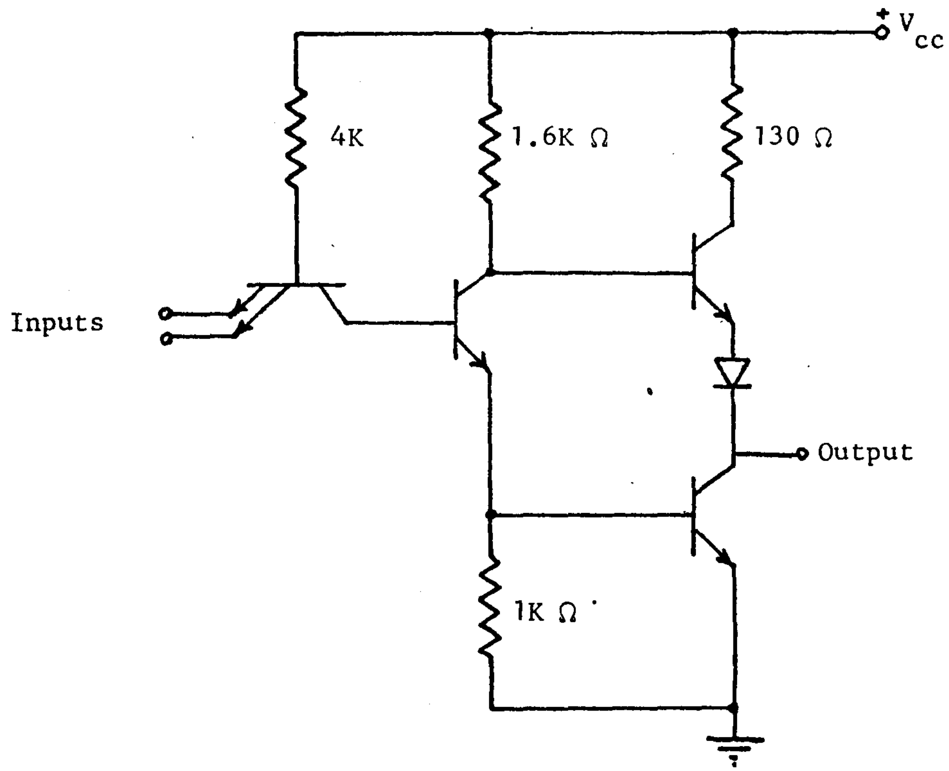


Fig. 6 (c). A Standard TTL Circuit.

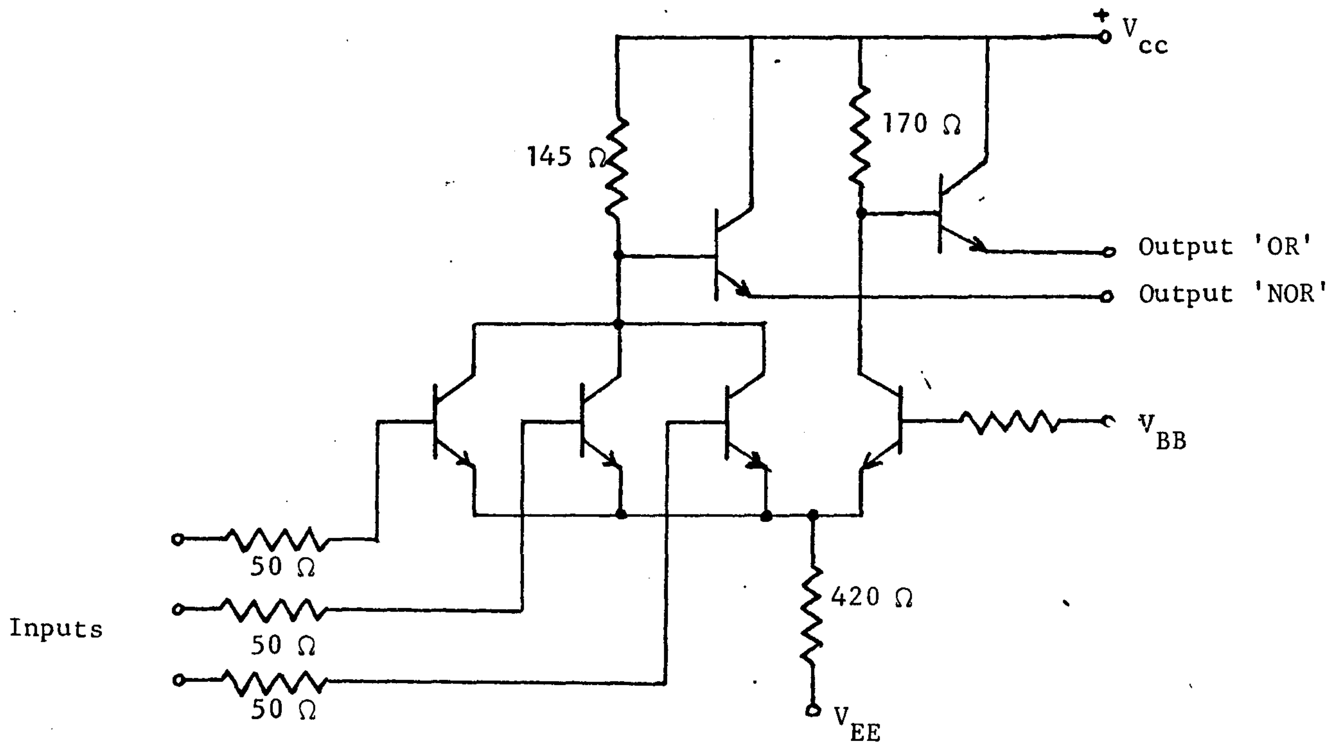


Fig. 6 (d). A Standard ECL Gate.

Fig. 6. Schematic Diagrams of Different Logic Circuits by Texas Instruments.

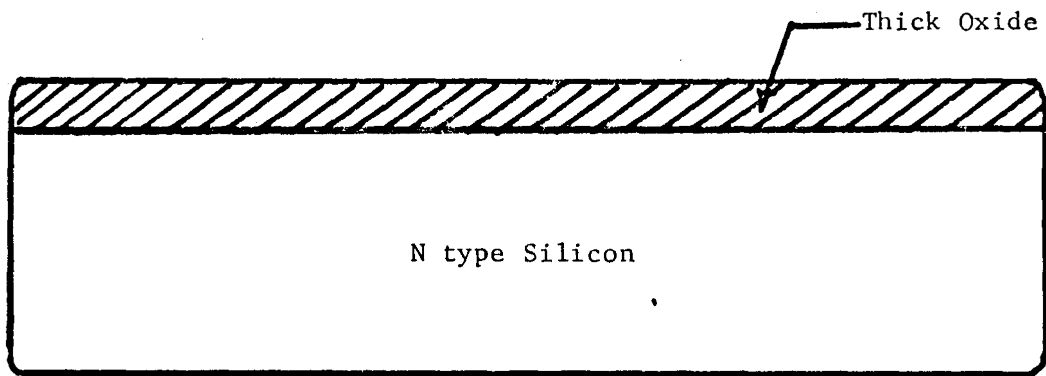


Fig. 7a. Basic Substrate

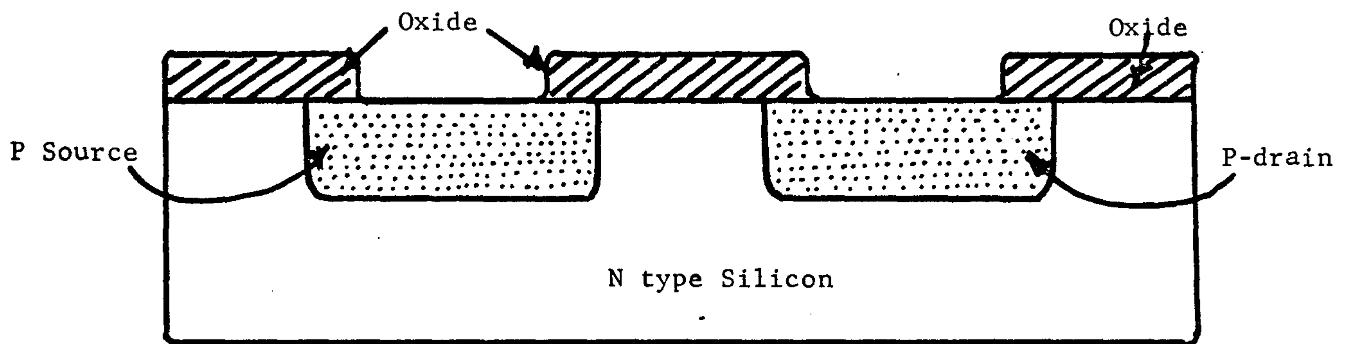


Fig. 7b. Oxide Etch-Source and Drain Diffusion

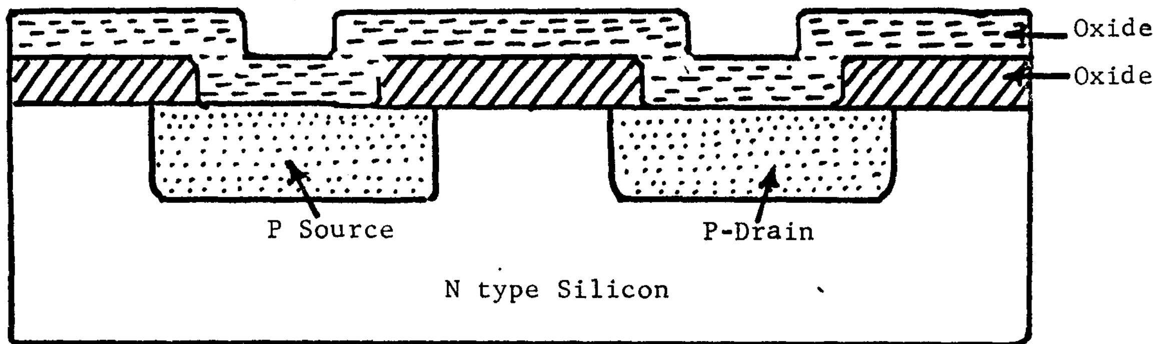


Fig. 7c. Reoxidation

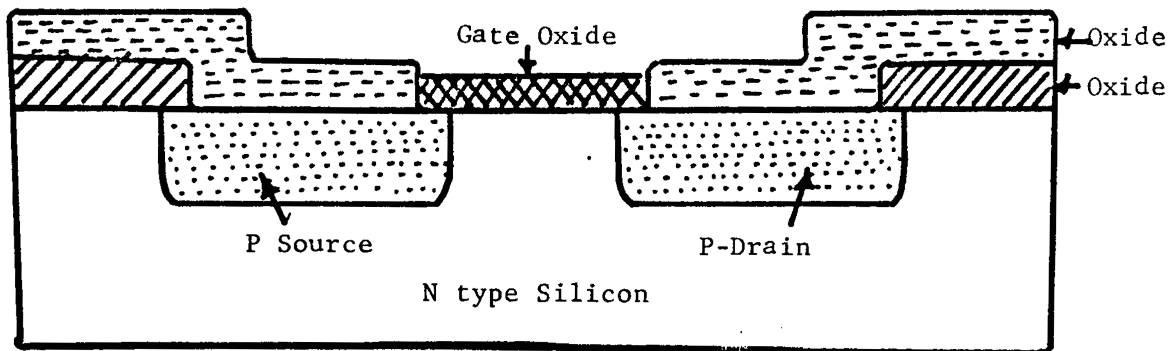


Fig. 7d. Oxide Etch-Growth of Thin Oxide Over Channel.

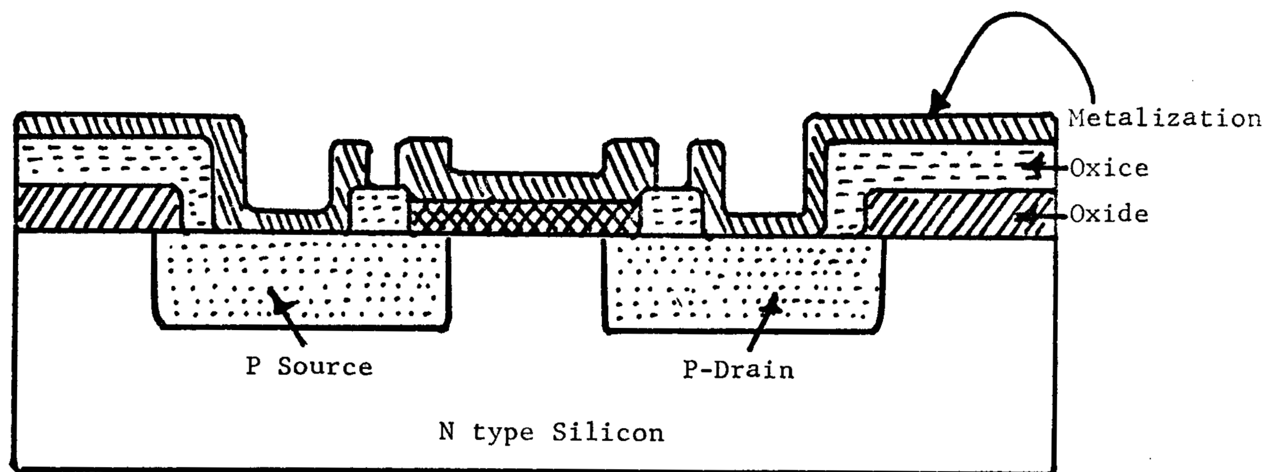


Fig. 7e. Oxide Etch and Metalization.

Fig. 7. Processing Steps in Fabrication of PMOS Structure.

$$V_T = \frac{X_o}{K_c}(Q_{ss} - Q_b) + \phi_{ms} + 2\phi_F$$

where

. Φms is the work function difference between the gate conductor and the bulk silicon

. F is the Fermi potential of the bulk silicon

. Qss is the fixed surface-state charge density per unit area

. Qb is the charge per unit area within one surface depletion region at the onset of strong inversion

. Xo is the gate dielectric thickness

. Kc is the dielectric constant of the gate insulator

. Co is the permitivity of free space

Therefore the threshold voltage of a device can be controlled by controlling any of the above parameters. On the basis of threshold voltage, MOS devices can be categorized under two headings. High Threshold devices like PMOS (P-channel MOS) having a threshold voltage of 4 to 6V and Low Threshold devices like MNOS (Metal Nitride Oxide Semiconductor) having a threshold voltage of 1.5 to 2.5V.

1. Efforts towards increasing speed

The speed of MOS devices can be increased by at least two techniques:

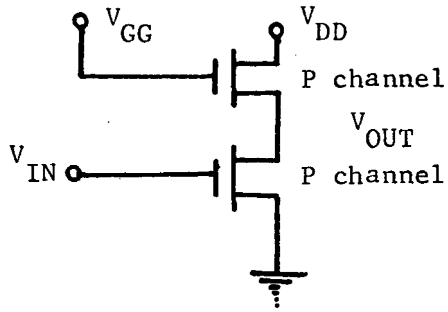
(1) by using different types of circuits - p-channel, n-channel, CMOS

(2) by using different techniques for doping silicon - like ion implantation as opposed to traditional diffusion method

The above two classifications are independent and one can have any combination of circuit type and doping techniques.

a. Types of MOS circuits

The different types of circuits that can be fabricated are shown in Figure 8 with Figure 7 showing different processing steps for fabrication of PMOS structure. Due to its ease of fabrication p-channel is the most commonly used structure. P-channel uses uses holes for conduction as against n-channel which uses electrons. The mobility of electrons being higher (approximately twice that of holes) n-channel structures provide faster circuits. As n-channel devices need to be only half the size of p-channel devices to achieve the same impedance level, n-channel devices have



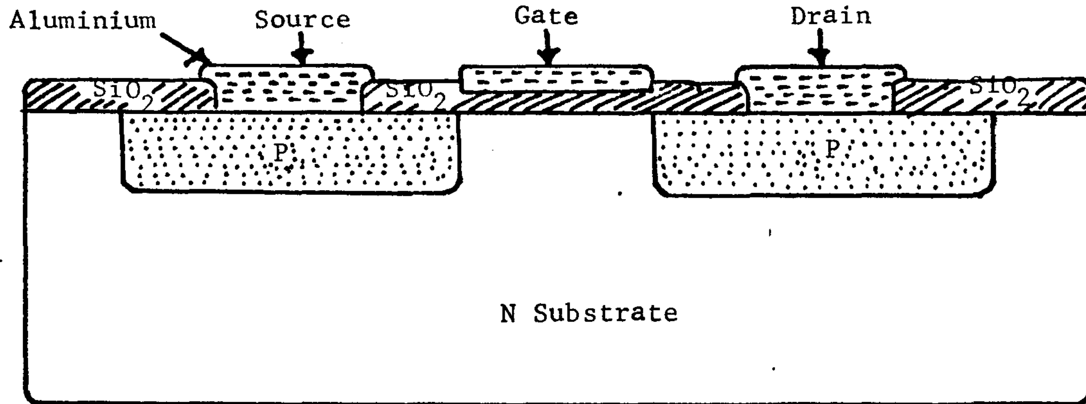


Fig. 8a. P-channel MOSFET with Circuit Schematic for a PMOS Inverter.

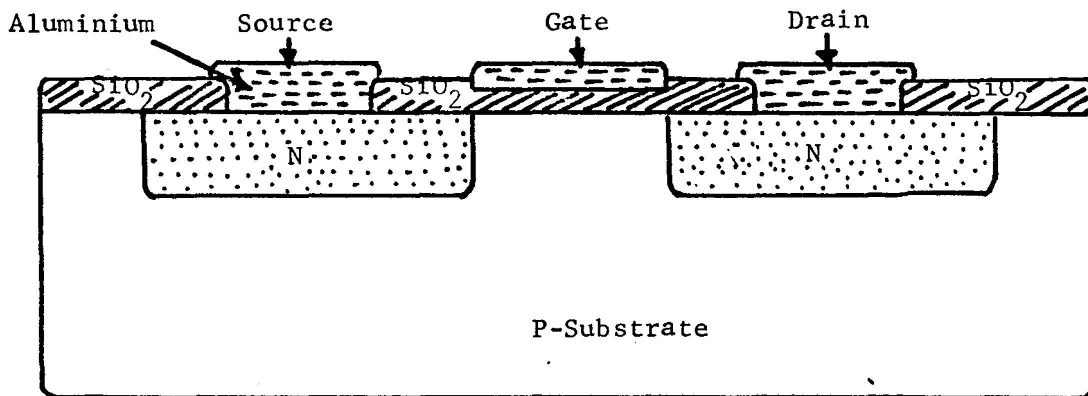


Fig. 8b. N-Channel MOSFET.

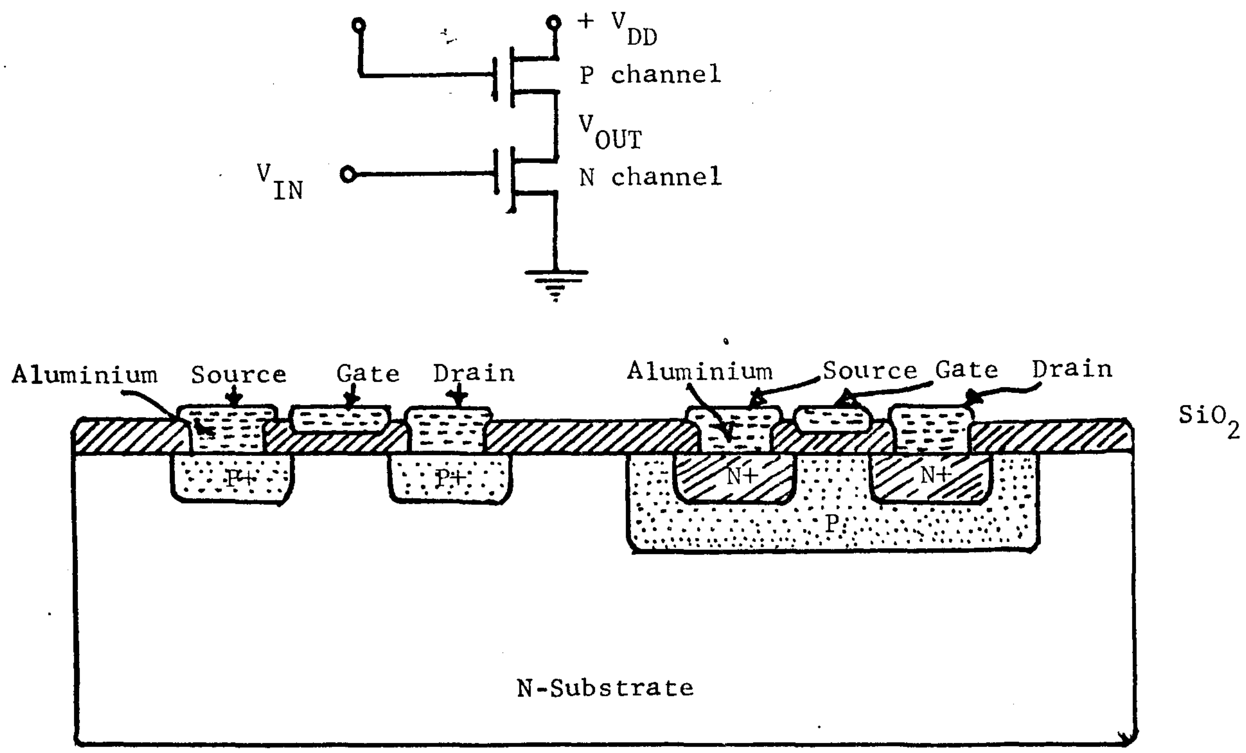


Fig. 8c. CMOS Transistor Structure with Circuit Schematic for a CMOS Inverter.

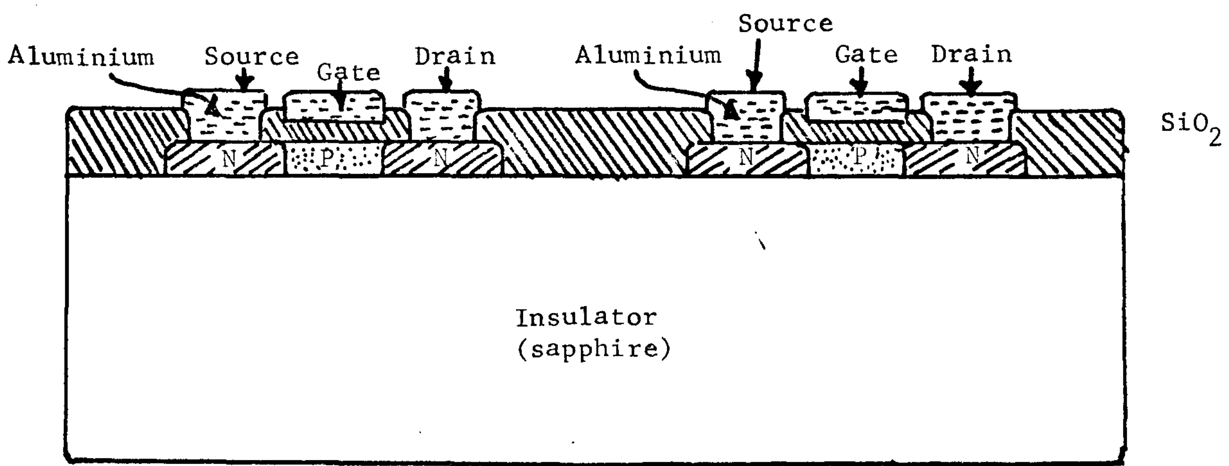


Fig. 8d. Silicon on Insulator Structure.

greater packing density. Even with all these advantages n-channel has not been able to compete economically with p-channel devices since the n-channel fabrication process is very difficult to control. The solution to this problem has been the CMOS circuit. This circuit is a series connection of p-channel and n-channel devices. The result is the formation of a circuit that has higher speed and near zero standby power. As the two devices are in series, in any condition one of them is off, producing a high impedance to ground. Therefore the power dissipation is only due to leakage currents. Also this circuit requires only one power supply, as against two in a single polarity circuit (see Figure 8a and Figure 8c). The disadvantages of this circuit are the fact that more steps are required in fabrication than in single polarity circuits thus reducing the yield, isolation between devices is required thus reducing density and the number of devices required to implement the same function is greater than in single polarity devices. Table 2 compares, among other things, p-MOS and CMOS devices. It should be noted that CMOS operates at a lower voltage (4-16V) thus making it more compatible with Bipolar than p-MOS (-27 and -13V).

b. Ion Implantation Technique

One of the reasons for the decrease in speed of MOS devices is due to the parasitic capacitances like gate to drain and gate to source capacitance. In diffusing source and drain using conventional techniques, the gate and source and the gate and drain have to overlap a considerable amount, so as to make an allowance for photomask registration tolrance. Ion implantation [Wilder , 1970] reduces these capacitances by means of better alignment.

The process of ion implantation is shown in Figure 9 for an MOS field effect transistor (MOSFET). As in the conventional case an n-substrate is taken into which source and drain regions are partially diffused. The gate electrode (which usually has a smaller width than normal) is then fabricated in the usual way. The whole chip is then subjected to a beam of Boron ions that are accelerated to high velocities. The electrons impinging on metal parts are collected harmlessly while the ones that strike SiO_2 pass through and dope the Si layer below. This completes the fabrication of the source and drain. It is easily seen that the gate-drain and source-drain alignment is automatic. It is estimated that this technique produces two to four times lower input capacitance and 40 times less Miller capacitance resulting in a device that is about five times faster than the equivalent diffused MOS transistor (Wilder, 1970).

2. Efforts towards compatibility with bipolar devices

Compatibility with the bipolar devices has been achieved by decreasing the threshold voltage of MOS devices. Such different approaches as crystal orientation of the Si, type of gate insulator used and the type of gate conductor used will now be discussed.

a. Crystal Orientation

The bulk silicon is characterized by a cubic crystal structure. The most common crystal structure chosen is one having Miller index (111). (Miller Index is defined in Runyan (1965), pp. 84.) It so happens that a lower threshold voltage can be achieved

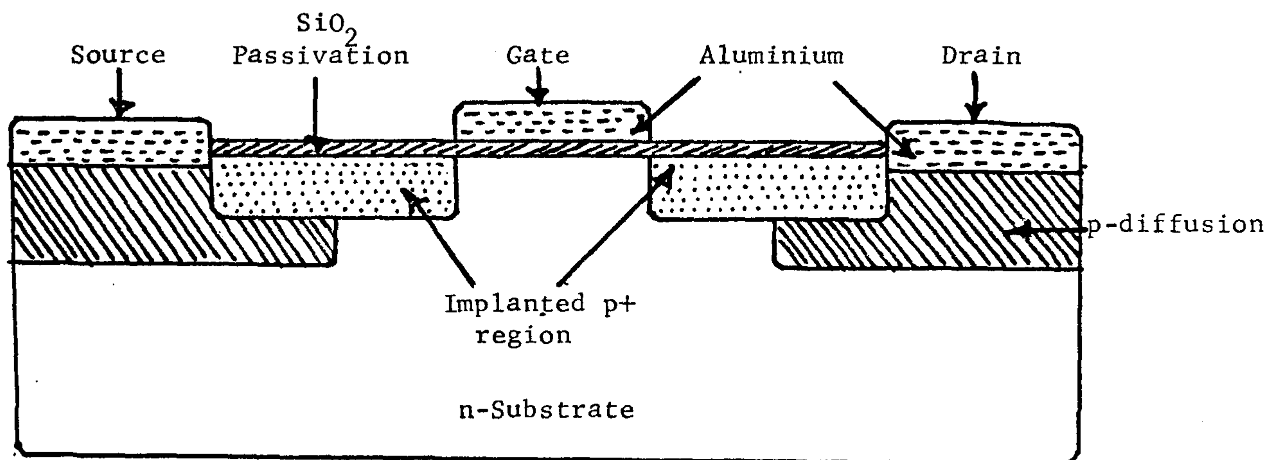


Fig. 9. A MOSFET fabricated using Ion Implantation.

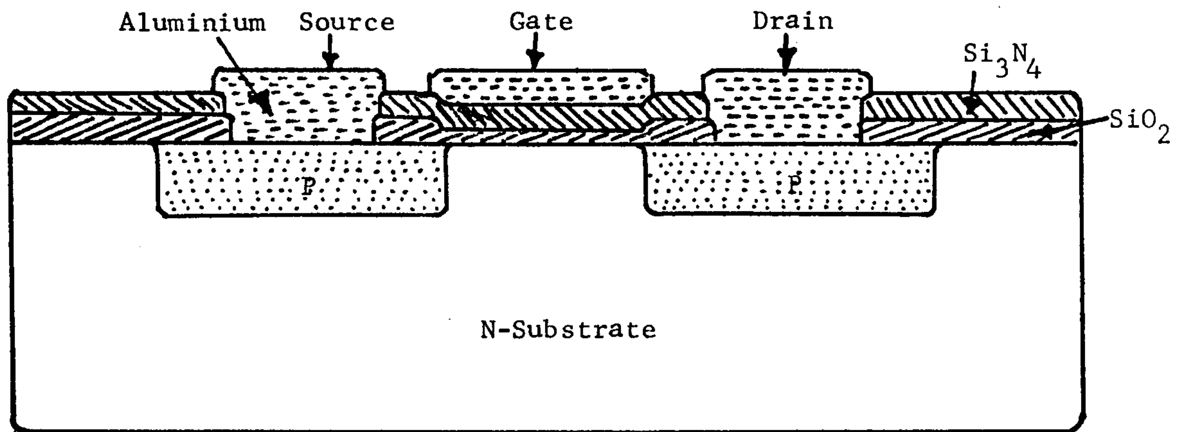


Fig. 10. Metal Nitride Oxide Semiconductor (MNOS) Structure.

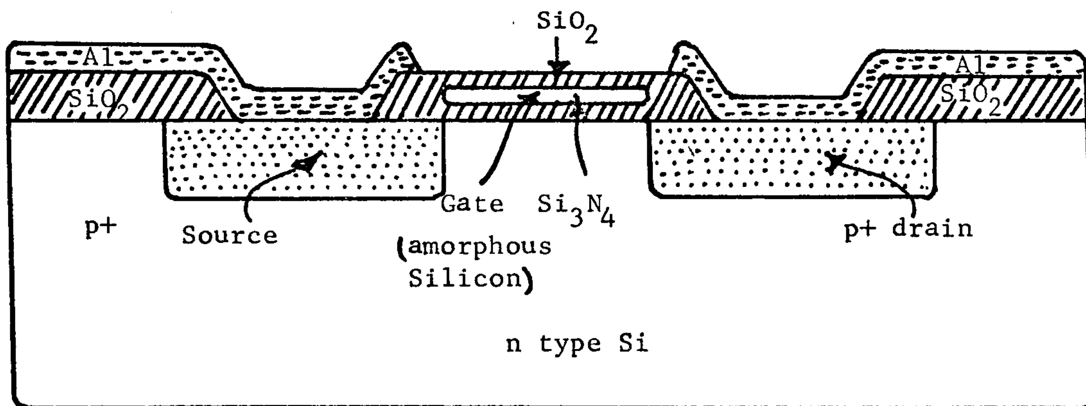


Fig. 11. The Structure of a Si-gate Transistor.

by means of using a crystal structure that is (100). A lower threshold thus brings about a closer compatibility with TTL circuits and lower power dissipation. The major drawback is that 100 structures bring about lower electron mobility, thus decreasing the device speed.

b. Type of Insulator

Traditionally the insulator used for fabrication of a MOS device has been SiO_2. Insulators with higher dielectric constants have been used to reduce the threshold voltage. The most popular material has been Silicon Nitride (Si_3N_4) but at times Aluminium Oxide (Al_2O_3) also has been used. The interface between Si and Si_3N_4 is difficult to control. Therefore a thin layer of SiO_2 is grown over the Si-substrate and Si_3N_4 is deposited on top of this. This produces a sandwich for the gate electrode. The result being an increase in dielectric constant for the same thickness of the dielectric. Figure 10 shows such a device which is known as Metal Nitride Oxide Semiconductor (MNOS).

c. Type of Gate Conductor

Since the inception of MOS devices Aluminium has been used as the gate conductor. The threshold voltage of a MOS device depends on the work function difference between the substrate and the gate conductors. This threshold can be regulated by choosing different combinations of the substrate and gate conductor. The work function for a p-channel Aluminium gate is estimated to be -0.3V (Wilder, 1970). Efforts have been made by different manufacturers to use Silicon and Molybdenum as gate electrodes. By controlling doping levels in these electrodes the work function can be controlled. In the following part a brief description of Si-gate and Moly-gate (Molybdenum gate) structures is given.

1) Si-Gate Structure

The technology as the name suggests uses amorphous silicon as a gate material. A cross section of the transistor with Si-gate is shown in Figure 11. The aim of lowering the threshold voltage is achieved in two ways. The first is by using SiO_2 and Si_3N_4 as the dielectric under the gate (MNOS) structure) and secondly by using a Si-gate. The gate electrode is made up of heavily doped p-type silicon. The combination of the dielectric and silicon gate brings the threshold voltage to 2V as against about 5V in Aluminium gate circuits.

The gate oxide is the most critical portion of an MOS transistor. In this process the gate oxide is covered up as soon as it is grown thus giving a high yield. As the alignment of gate-source and gate-drain is not difficult the parasitic capacitances are smaller and the Si-gate transistor can operate at a faster speed. There are three layers of interconnection possible, namely Diffused interconnection, Aluminium interconnection and Silicon interconnection. These together with the smaller dimension of the transistor bring about a high density of devices. Finally the greatest advantage of this process is that the device produced is directly compatible with Bipolar devices. For more detail on this the reader is referred to the paper by Vadasz et al. (1969).

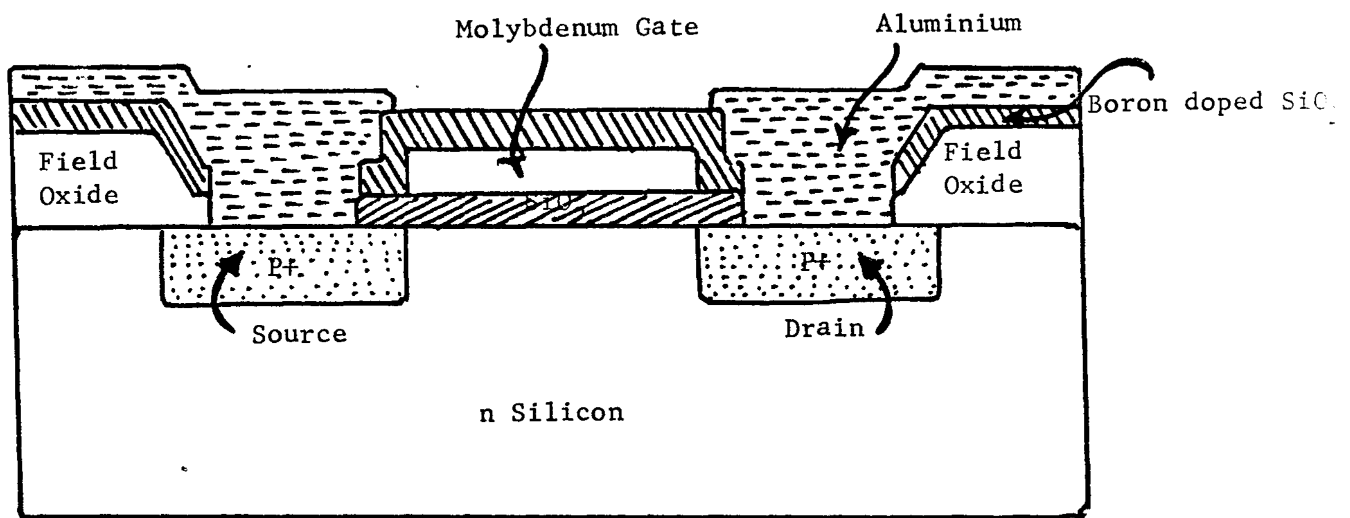


Fig. 12. The Structure of Molygate Transistor.

	p-MOS on <111>	p-MOS on <100>	Si-gate	MNOS
threshold voltage	4-6V	2-2.5 V	1.8-2.2 V	1.5-2.5 V
relative feedback capacitance	4	4	1	6
relative packing density	0.7	0.7	1	0.7
threshold voltabe of field oxide	25 V	16 V	25 V	25 V

Table 3. A comparison of different fabrication processes for MOS devices (adopted from Wilder (1970)).

An example of a chip produced using this technology is Intel's 1101, a 256 bit random access memory. This has all inputs and outputs compatible with standard TTL and DTL inputs.

It is believed that as the industry matures this will be the most widely used technology.

2) Molybdenum Gate Structure

The next innovation after Si-gate was the Molybdenum gate (Moly-gate) which not only reduced the threshold voltage but also improved the speed of MOS devices. The basic features of molybdenum are its high melting temperature, good match of thermal expansion with Silicon and high electrical and thermal conductivity. The process starts with an n-type silicon chip on which a 1.3 micron thick field oxide is grown . (Figure 12 shows a molybdenum gate device.) Part of the thick oxide is then etched away wherever source, drain and gate are to be formed. A 0.1 micron gate oxide is then grown in these areas and molybdenum is deposited over the whole surface. Then molybdenum is etched away selectively in areas where source and drain have to be formed. Glass doped with Boron is now deposited over the entire area. The chip is then treated to 1100 degrees C so the Boron diffuses into the n-silicon to form the source and drain. The molybdenum and field oxide act as aligning entities producing a minimal gate to source and gate to drain overlap. This decreases the parasitic capacitance improving speed. Finally contact holes are etched and aluminium deposited.

In the Si-gate process the gate conductor and p-region diffusion, which are performed simultaneously, have to be carefully controlled. Excessive diffusion may cause reduction in threshold voltage below the minimum value where as too little diffusion may cause high threshold voltage. In the molybednum gate process the gate conductor is not diffused. This allows a simpler fabrication technique thus increasing yield. Molybdenum has a melting point of 2600 degrees C and can easily survive the 1100 degrees C temp. for diffusion of Boron. Molybdenum also has a low sheet resistance (0.15 ohms per square) and hence the gate does not produce excessive voltage drops.

With all the above features it seems that Molybdenum gates have a distinct advantage in self-aligning and high-temperature chip assembly over Aluminium or Silicon gate technology. These devices occupy about 20 percent less area than conventional devices (Laughton, 1971). The General Electric Company, Syracuse, has produced a 100 bit dynamic shift register (GER 1507) which is compatible with standard TTL and DTL circuits and capable of working at 5MHz. Also, a 4096 bit RAM with cycle time of 125 nsec. is being built (Laughton, 1971).

All the above processes indicate that the trend of the technology is to introduce high speed circuits compatible with Bipolar retaining the advantages of MOS fabrication. Table 3 taken from Wilder (1970) shows the different parameters of the above processes. As more experience is being gained in the MOS industry it should not be long before a few standard fabrication techniques become dominant.

III. MOS OR BIPOLAR FOR LSI

Large Scale Integrated circuits are currently fabricated using one of two basic device technologies as reflected in the preceding discussion on manufacturing processes. The technologies are Bipolar and MOS; each of which has advantages and disadvantages. As the technologies develop and new designs of processing and fabrication are introduced the advantages of one over the other will be diminished. Since the technologies are changing very rapidly, any long term comparison between them is obsolete within about six months (Warner, 1967).

One of the earliest discussions on MOS vs. Bipolar was presented in a paper by Warner (1967). Another good reference for a comparison of technologies is a book by Khambata (1968). Most of the discussion in this part of the paper has been taken from the above two works.

The fundamental difference between the Bipolar devices and MOS devices is the fact that Bipolar transistors are minority carrier devices whereas the FET is a majority carrier device. When one looks at the external characteristics of the two transistor types, the FET characteristic is more akin to vacuum tube than the Bipolar transistor. The input impedance for FET devices is large whereas for Bipolar devices it is small. The output impedance for both devices is large.

In choosing the fabrication technique for these devices many factors are usually considered: on one hand there is a need to satisfy the user requirements, viz. the operation time (often called switching time), power consumption, number of circuit types available etc. These have already been discussed in a previous section. On the other hand there are certain restrictions on the manufacturer for favoring a choice of one technology over another. Some of these factors are: the ease of fabrication; the number of manufacturing steps involved; the area required to fabricate a transistor, a resistor and a capacitor on the chip; the area required for interconnection between circuits; the problems associated with isolation between circuits; the possible yield, etc. A summary comparison of the above factors is shown in Table 4 . It can be seen that when fabrication and device density are considered MOS has a distinct edge over Bipolar; but Bipolar devices are much faster than MOS. The following sections will develop these contrasts in more detail.

A. SPEED CONSIDERATIONS

In designing LSI circuits using MOS or bipolar devices one of the main considerations is the speed of the device. In a bipolar device the speed is dependent upon the parasitic resistances and capacitances which are present at the various junctions (emitter-base junction, collector-base junction). Speed also depends upon the movement of the minority carriers through the various regions of the transistor. The load capacitance occurs in parallel with the junction capacitances. It is found that (Warner, 1964) the charging time for these capacitances is much higher than the base transit time and hence the former dominates in determining the speed of these devices. In the case of FET's there are no transit time delays and the speed is dependent upon the delays due to resistance and capacitance present in the circuit.

	Bipolar	FET
Kind of Carrier	Minority	Majority
Input Impedance	Small	Large
Output Impedance	Large	Large
Type of Device	Unilateral	Bilateral
Major steps in making a device	usually 3	usually 1 (induced channel) sometimes 2 (diffused channel)
Difficulty in fabrication	145%	100%
Major number of steps	130	38
Area required by devices	Large	Small
Area required for interconnection	Large	Small
Area required for one device	24 mil^2	1 mil^2
Sheet resistance for resistors	200-250 Ω	4000-50,000 Ω
Metal to silicon contacts	3	2
Transconductance	Large	Small
Frequency response	Larger	Smaller
Power dissipation	Large	Small
Interface requirement with existing circuits	no	yes
Speed	Fast	Comparatively slow

Table 4. A comparison between Bipolar and MOS devices (circa late 1968 but relative values are not expected to change).

Hence the transconductance of a device is the most important parameter in the response time of a device. It is generally found that the transconductance of a MOS device is much smaller than that of a bipolar device. This simply means that the delay due to a bipolar device is much smaller than a MOS device. Warner (1967) considers $g_m/\sqrt{C}$ as a figure of merit (where g_m is the transconductance and C is the total lumped capacitance associated with a circuit) and shows that bipolar devices have an inherent advantage of about 65 over the FET. It should be noted that the transconductance of bipolar devices is technology independent whereas that of MOS devices is technology dependent. This generally means that as the technology improves the MOS devices should become faster and faster and compare more favorably with bipolar devices.

B. SPEED-POWER CONSIDERATIONS

In integrated circuits (IC's) one cannot look only at the speed of the device but some consideration must also be given to the power consumption. In certain circuits it is possible to trade speed for power. However, if power dissipation is excessive, then the number of circuits that can be packed in a given volume are limited. As the power dissipated in an integrated circuit increases it may cause a gradual change in device characteristics or reduction in useful life or catastrophic failures. This affects the reliability and performance of IC's. In LSI, where there is a continuous effort towards making circuits as fast as possible together with packaging them in as small a volume as possible, a figure of merit is required which considers both speed and power consumption of the circuit. Such a figure of merit for a digital circuit was defined by Joseph (1965). He considered the product of the signal propogation delay and the static power requirement of the circuit. The speed-power figure of merit is the reciprocal of this number. Joseph (1965) shows that the bipolar circuits have a speed-power advantage of at least 15 over that of the FET circuits. Warner (1967) distinctly shows that if the above figure of merit is considered, then bipolar devices have a distinct advantage over the MOS devices.

C. DEVICE DENSITY CONSIDERATIONS

If one compared the device density of Bipolar and MOS on integrated circuit chips, it would be found that MOS devices require an area that is much smaller than the Bipolar. This is essentially so because

(1) the area required for a transistor is smaller for MOS. The interconnection pads, the insulation width, etc. are also smaller.

(2) For a given resistor value, the area required for MOS is smaller than for Bipolar, since the surface resistance of MOS devices is higher.

(3) To perform the same function MOS circuits require fewer elements than the Bipolar circuits.

All the above facts give an indication that MOS devices will have a much higher density than Bipolar.

D. INTERCONNECTION AREA CONSIDERATIONS

Another consideration in LSI applications is the interconnection area requirements. Two distinct kinds of areas must be considered:

(1) the metal pads for connection to the outside world

(2) interconnection of devices on the same chip.

When the chip has a circuit which is substantially simple , the total chip area is mainly governed by the metal pads. In such a case MOS and Bipolar devices will naturally consume nearly the same area. On the other hand, when the circuits are very complex with a large number of devices the area taken up by the pads does not constitute a significant part of the chip area and hence under such conditions MOS devices have an advantage.

In the second case, where interconnection patterns are required for connecting different elements on the same chip, MOS also has an advantage. The MOS circuits are usually operated at higher voltages and lower current values than the Bipolar circuits and therefore the metallic area required for innerconnections is smaller.

All the above reasons bring about a smaller total interconnection area requirement for MOS than for Bipolar.

IV. INTERCONNECTION METHODS

The introduction of integrated circuits into the market created a serious problem for the manufacturers. The problem consisted of meeting all the customer requirements while maintaining the economics of large volume production. This was quickly solved by marketing two kinds of products. One was the standard circuits like the NAND gates, inverters, shift registers, etc. The others were the custom designed circuits. In LSI, where the number of circuits per chip is large the above problem became more severe. Except in the case of memory circuits the number of parts required by the customer were numerous and hence the manufacturers started looking for methods that could allow them to produce custom designs at a low cost and with quick turn around time. Different methods were proposed by different manufacturers. Some of these methods were:

(1) The Discretionary Wiring approach of Texas Instruments which was based on the economies of increased yield of a circuit

(2) The Micromatrix apporach of Fairchild which was based on maximizing the standard number of production steps for LSI chips, thus achieving the economies of batch production

(3) the Polycell approach of Motorola which used Computer Aided Design (CAD) together with the batch production techniques mentioned above

(4) Other approaches: There were other approaches proposed by different manufacturers which have yet to gain a wide popularity.

The Discretionary wiring approach falls under the general name of Random Interconnection Pattern (RIP) whereas the Micromatrix and Polycell approaches are Fixed Interconnection Pattern schemes (FIP). The above three approaches will be described briefly in the following paragrpahs.

A. DISCRETIONARY WIRING APPROACH OF TEXAS INSTRUMENTS

In using this approach a chip is produced with more devices etched on it than are required for the logic function. On this chip a first level of metallization is done irrespective of whether the devices have some defect or not. At appropriate places metallic pads are also deposited to carry out a multiprobe test. The result of this test would indicate the good and bad cells on the chip. This information together with the functional requirement of the chip is then fed to a computer. Using this data, a computer program then generates the required information for the second and the third levels of metalization. This information is then fed to a Cathode Ray tube through a D/A (digital-to-analog) converter. Photomasks for the second and third levels of metallization are then produced using the face of the Cathode Ray tube. Figure 13, adopted from Khambata (1968), gives a block diagram of the Discretionary Wiring Approach.

The Discretionary Wiring scheme has a very high yield and the amount of testing

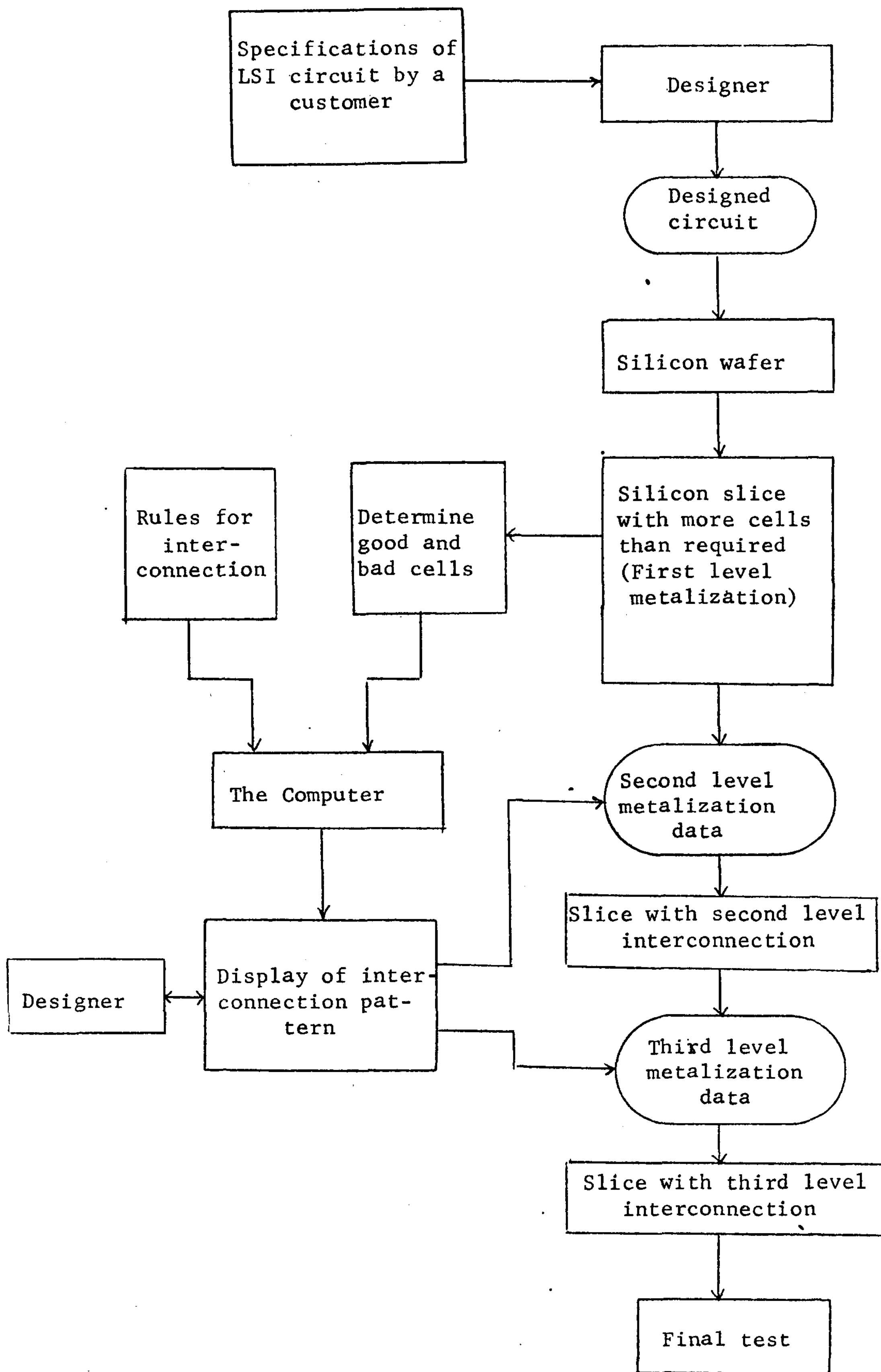


Fig. 13. Design steps in the Discritionary Wiring Approach (adopted from Khambata (1968)).

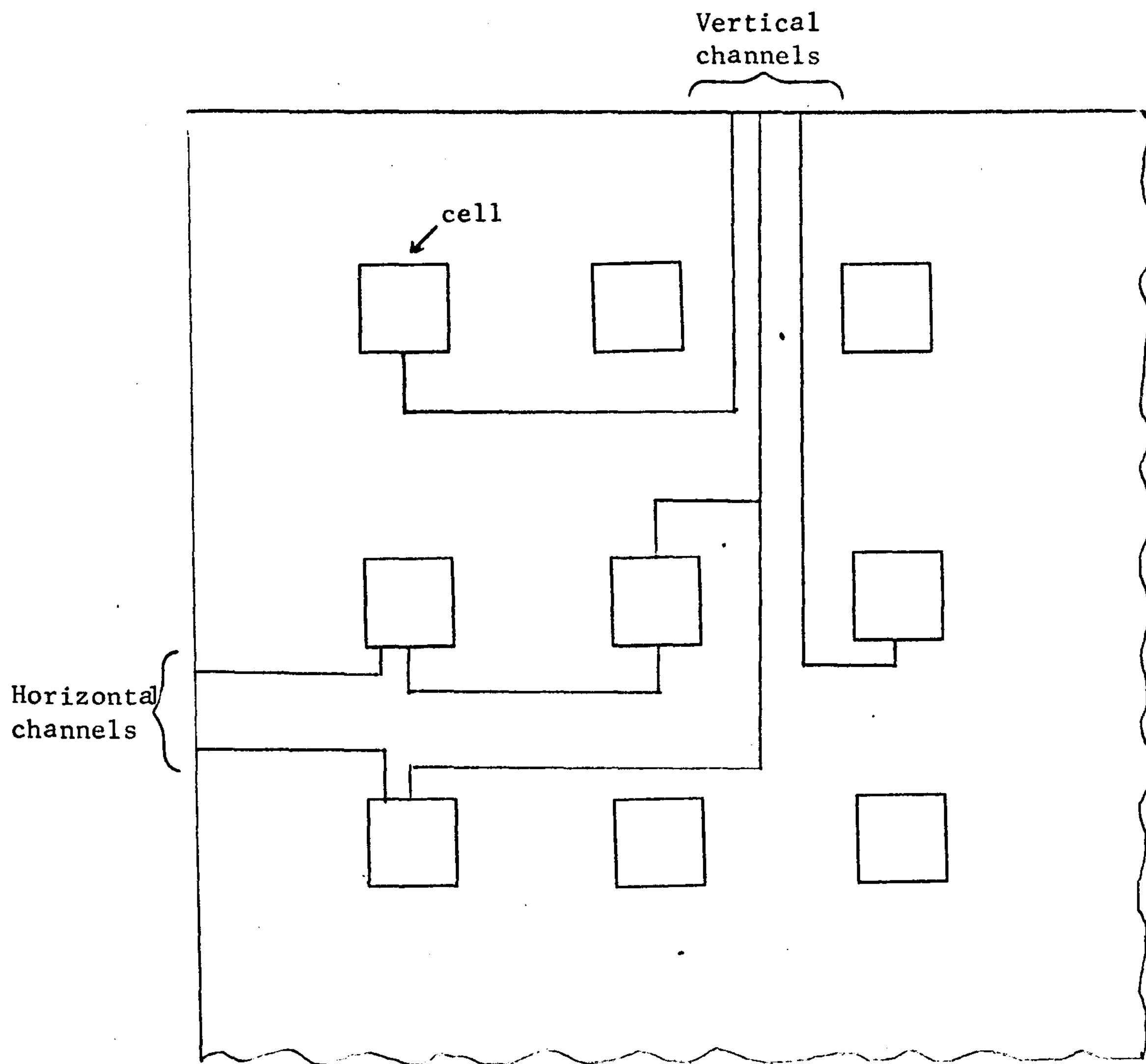


Fig. 14. The master slice for fixed interconnection pattern showing vertical and horizontal channels.

required at the final stage is significantly reduced. However, there are a number of drawbacks. The major ones are:

(1) The effective density of devices on the chip is reduced. This is due to two factors - the requirement of test pads and the etching of redundant devices on the chip.

(2) Even though the first level of metallization is tested the second and third level of metallization may also have faults resulting in a rejected chip.

(3) The computer program for the second and third level masks must be able to handle all the different device configurations on the first level. However, this program should require only a reasonable amount of computer time as the cost of this step should remain within limits.

Finally, as stated by Petritz (1966), it should be noted that "if one has 100 percent yield over the area of the slice to be used, the probing test is eliminated. Also the computer program for pattern generation will be somewhat simpler because the location of gates is known." If this happens then the Discretionary Wiring scheme is the one that is most desirable, but the probability of a defect free silicon slice is quite small at present.

B. MICROMATRIX APPROACH OF FAIRCHILD

This approach is a specific example of Master Slice Fixed Interconnection Pattern (Master Slice FIP) method. In this approach the circuits share all the masks except for those involved in metallization. Figure 14 shows a conceptual diagram of this scheme in which there are certain areas reserved for cells and others reserved for interconnection. These are called vertical and horizontal channels. The Micromatrix approach consists of chips with arrays of cells having different functions (like NAND gates, FF's, etc.). These arrays are chosen so that they can satisfy a given customer requirement. The arrays are prefabricated and stocked. Prefabrication allows batch production. Thus the assembly line can be studied and volumes of data can be gathered to predict reliability and failure mode.

When a customer requests a design, the design is analyzed and an appropriate chip with an array of cells is chosen. Pads for input/output are then allocated and the first level metallization is designed. On top of this layer an insulating layer is required before a second level of metallization can be made. Vias (holes in the insulation layer to connect the first and second level of metallization) are selected and a second level metallization pattern designed. All this is done by a designer and a draftsman using special design layout sheets. After the layout is completed the artwork is used to make a set of photolithographic plates to produce the required masks.

This interconnection scheme is very attractive but has some inherent drawbacks. In this scheme automatic design methods are not exploited to save human error and human labor. Also the number of types of cell arrays that can be stocked is limited.

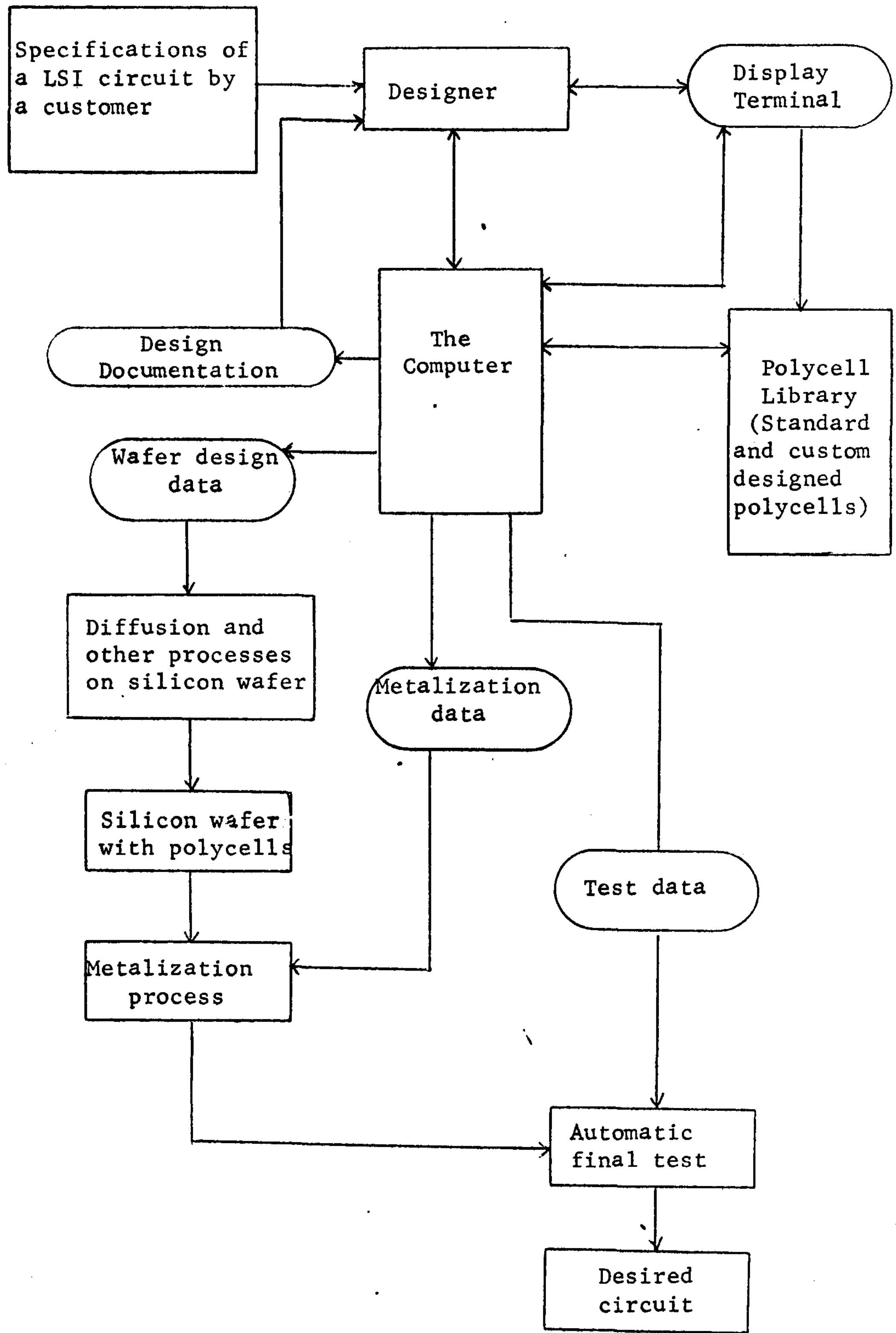


Fig. 15. Design steps for Polycell Approach (adopted from Khambata (1968)).

Overall this scheme has some attractive features and looks more promising than the Discretionary Wiring approach.

C. POLYCELL APPROACH OF MOTOROLA

This approach exploits Computer Aided Design (CAD) method to lay out the interconnection patterns for LSI chips. Initially, a library of cell designs is maintained inside a computer memory. These cells are commercially called Polycells by Motorola. The Polycell inventory is changed as new designs are encountered. When a custom design is required a design engineer analyzes the requirements and, with the use of a display and teletype, communicates with the computer. He can select different Polycells to be laid out on a chip and display them if required. Simultaneously, data structures are generated inside the computer to depict the layout of the cells. When the design is finished the computer can generate instructions for an automatic drafting machine to prepare the complete set of mask masters for the array. Figure 15, taken from Khambata (1968), shows the design steps in the polycell approach.

The outstanding advantage of this scheme is the great flexibility that a designer has in choosing the polycells by interaction with the computer. Due to CAD the turn around time is minimized. An optimum design can be accomplished since the computer keeps track of the complexities which, if designed by a human, would present a formidable task. Besides, a customer can define his own Polycells, which, if proprietary information, can be guarded very easily. For a particular design, there is a possibility of combining two or more Polycells to achieve power reduction, increment in speed or higher density or other such advantages. Even though computer time is costly, changes in design are not formidable and are easy to make. The designs could also be checked exhaustively by the computer before fabrication. All of the above points make the Polycell approach the most attractive of the three described. If Motorola can deliver all that is claimed in the above approach, then this scheme would be the most reliable and economical to use.

D. OTHER APPROACHES

Other possible approaches like the Programmable Interconnection Techniques (McKintosh, 1964), Pad Relocation Technique developed at Hughes Aircraft (Calhoun, 1969), Yield Optimum Array developed at Westinghouse (Sack et al., 1964), etc. are not as common and hence are not discussed. If interested, a reader may consult the references indicated.

Finally, to summarize, it can be said that interconnection is the crucial problem in LSI. The percentage yield, density of devices, and the cost of LSI circuits is very heavily dependent upon a choice of the correct interconnection technique. Of the major approaches discussed above it remains to be seen which one will gain widespread acceptance.

V. PACKAGING

Packaging is necessary for LSI chips because:

(1) interconnection between chips can then be accomplished

(2) the devices that are etched on the chip could be protected from different types of ionic contamination which reduce the life or change the properties of the devices

(3) the heat dissipation problem is reduced by using a heat sink

(4) chips can be held for insertion into printed circuit boards.

The material used for packages is of three different types: Glass-metal, Ceramic, and Plastic. The plastic packages are a more recent advancement and are essentially much cheaper than Ceramic packages. The different kinds of packages are distinguished by their shapes. Some common types are Radial lead, Flat Packs, Dual-In-Line (DIP's) and Multichip packages. Figure 16 shows construction details of three package types.

The radial lead packages are usually made of glass and metal. Commercially they are known as TO-5 and TO-18. The TO-5 and TO-18 structures are very similar except that TO-18 has a smaller structure than TO-5. The number of pins that are available on these packages varies from 2 to 12. Thus they are very pin limited. The flat-packs are produced both in rectangular and round shapes. Flat-packs are light-weight and used extensvely in the aerospace industry. But these packs are relatively costly. Hermetic sealing problems have been encountered with flat-packs. TI has a family of flat-packs with 16, 24, 28, 36, 40 and 50 leads. Dual In Line Packages (DIP's) are the most popular package of those described. These packages are best suited for automatic insertion and it is expected that they will be widely used for a long time. The most popular DIP's are in 16 and 24 pin sizes even though there has been talk about 50 or so lead flat packs and DIP's. The most popular spacing between the pins is 100 mils and 600 mils center to center and it seems that this may remain so for some time to come. This pin spacing allows the assemblers and inspectors to work with the package without requiring magnification. (EDN Staff, 1970) There was a proposal for Quad in Line Package (QUIP's) which retained the 100 mils center spacing and increased the number of pins by having four rows and staggering the pins.

The DIP's or QUIP's may slowly overcome the large pin requirements for LSI but they have other disadvantages. There is stress on the seal at the corners and this may cause problems. Secondly, when these packages are used for very high speed logic they may not satisfy the speed requirements. The delay in getting into and out of the package may be significant. Also DIP's (as well as flat packs) take up too much real estate on a board and cost too much (Rostky, 1971).

IBM, which is the largest manufacturer of MSI and is expected to be a large manufacturer of LSI has an entirely different type of package. It has square ceramic

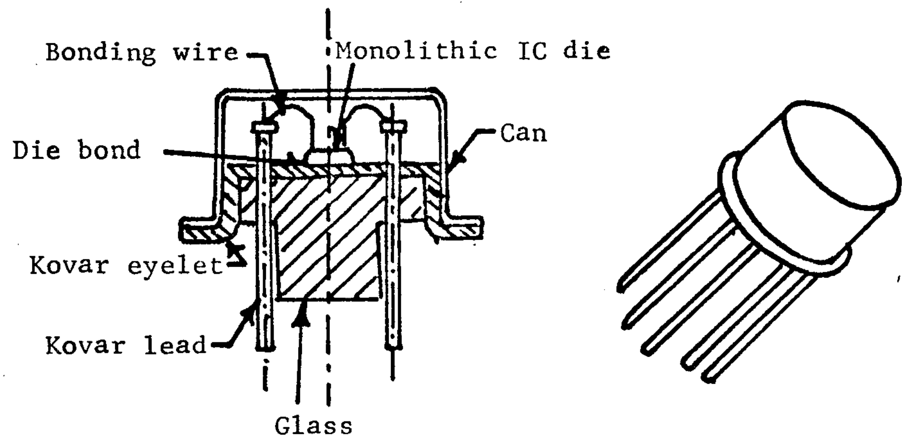


Fig. 16a. TO-5 IC Package

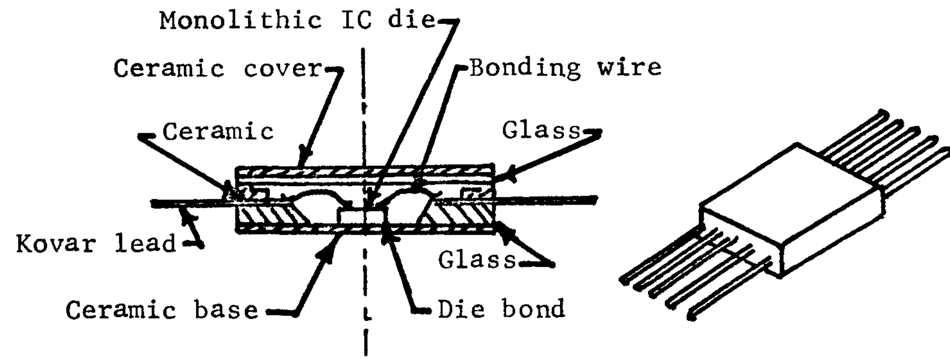


Fig. 16b. Ceramic IC Flat Package

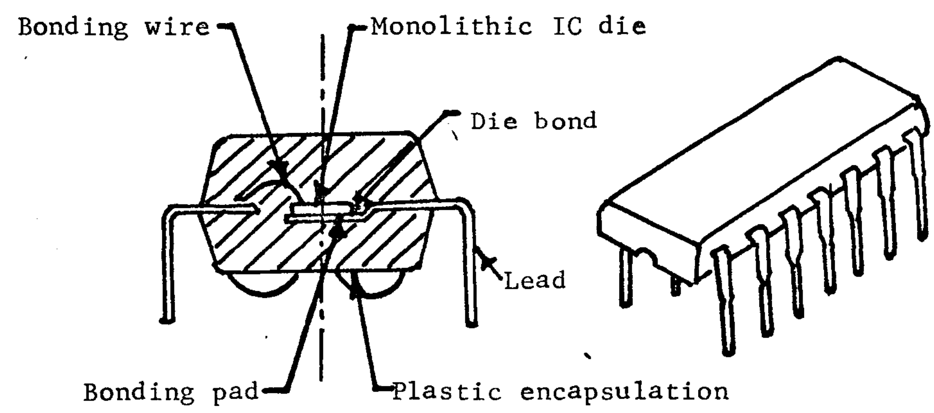


Fig. 16c. Plastic Dual In Line Package

Fig. 16. Construction Details of Different Packages.

substrates with 28 pins coming out of the bottom. There are other types of packages emerging in the market which are not yet well known. Some of these are the edgemount packages and leadless ceramic packages.

For the near future the most common packages will be ceramic or plastic with an average of 40 pins. The DIP is the most popular configuration today and it not only houses chips but also passive components. This trend will remain prevalent for the next few years. For complex functions, multichip packages may be used in which a number of LSI chips are inserted inside a package.

Finally, Bryant C. Rogers (the father of the dual in line package) in talking about today's packaging industry claims that "There is a clear need for revolt, for constructive creativity in interconnection hardware and semiconductor enclosures, which will not detract from the economies and performance of semiconductor IC's" (Rogers, 1972).

VI. SEMICONDUCTOR MEMORIES

Over the years the cost of processor elements has steadily decreased, making the memory a dominant factor in the cost-effectiveness of a computer system. Processor performance has also been limited by the memory speed and hierarchy of organization. Traditionally computers have used magnetic elements for data storage. However, in the last few years, semiconductor random access memory components have been introduced as scratch pads and small buffer memories where the cost-performance advantage of fast memory systems is the greatest. More recent developments in LSI technology have resulted in semiconductor Random Access Memories (RAM's), Read Only Memories (ROM's), Programmable Read Only Memories (PROM's) and a multitude of other types that are competitive in cost-performance to the traditional core memories. Examples of the emerging applications of LSI to main frame memories are in such large systems as the IBM 370/145, Illiac IV and in such medium scale systems as DEC PDP-11/45, Data General Supernova SC.

A. THE INTERFACE PROBLEM

When using magnetic core memories interface circuitry is required between the digital logic and the memory. The signals used by the processor logic and the memory are incompatible. Therefore interface circuitry is used to generate and decode signals used by, and received from, the memory. The high cost of the interface electronics places economic restraints on the system organization. Semiconductor memories, however, remove these restrictions since they can use the same types of components and fabrication techniques as the processor logic. Currently the most common type of circuity used in the processor has been TTL. Not all the different semiconductor memories types are compatible with TTL logic. For example MOS technology uses entirely different logic levels. But the trend has been to offer signal levels compatible with bipolar logic circuits. Even in cases where some interface circuits are needed (as in dynamic MOS) the complexity and performance requirements for these interface circuits are less severe than for ferrite-core interface circuits [Graham 1970].

B. CLASSIFICATION OF SEMICONDUCTOR MEMORIES ACCORDING TO DEVICE TECHNOLOGY

Semiconductor memories can essentially be classified under two major headings.

(1) Bipolar Memories

(2) MOS Memories

1. Bipolar Memories

Bipolar memories are faster than MOS memories. Bipolar devices make the best memories in the speed region of 100 nsec. or faster cycle time. Bipolar memories are being built and delivered in substantial quantities. The Illiac IV memory is specified at

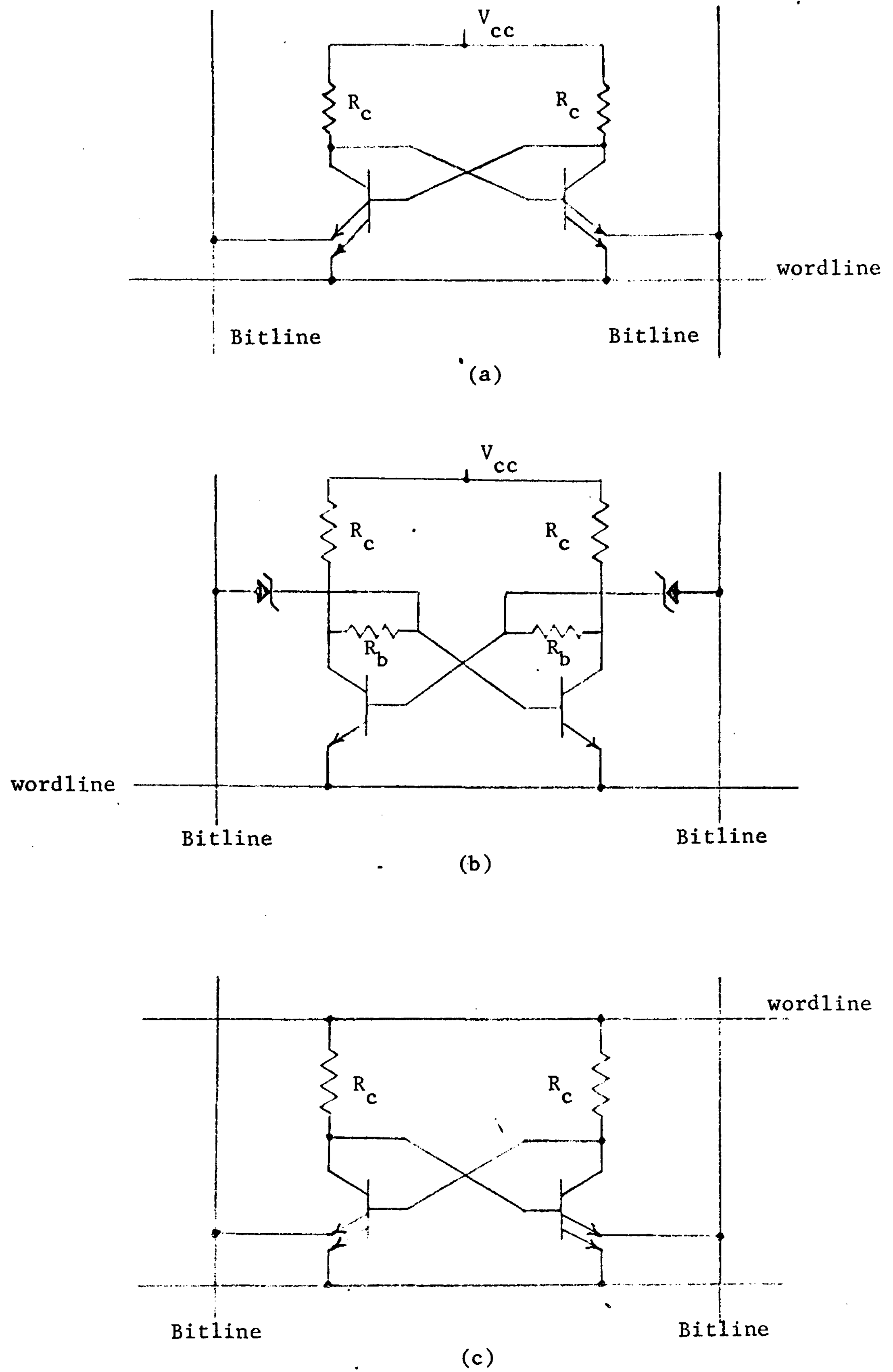


Fig. 17. Bipolar Memory Cells

(a) Simple Dual Emitter Flip Flop
(b) Flip Flop with Schottky Diodes
(c) ECL Flip Flop

200 nsec. cycle and 188 nsec. access times. The basic building block is a 256 bit bipolar chip 115 mil x 147 mil in area. The PDP-11/45 processor also uses bipolar memory with 300 nsec. cycle time. These memories are also being used for buffer or scratch pad applications. The greatest disadvantage of these memories is that high yields cannot be obtained with current fabrication techniques and the power dissipation is higher than for MOS memories.

Three different types of bipolar memory cells are depicted in Figure 17. Fairchild's 256-bit RAM, from which the Illiac IV memory is built, uses a basic circuit like that shown in Figure 15a. A particular memory cell may be selected for either writing or reading by applying proper signals to the word and bit lines. The word line voltage is raised to read the contents of a cell. The flip-flop current that normally flows through the word line transfers to one of the bit lines. A current sensing amplifier detects the signal current. Similarly, for a write operation the word line is raised and the two bit lines are suitably unbalanced to force the flip-flop into the desired state. When the word line is low the bit lines do not affect the cell state.

Intel's 256-bit RAM uses the circuit shown in Figure 17b which incorporates two additional gating Schottky diodes to achieve faster switching speed. The read operation is similar to that for the cell using dual-emitter transistors. When writing, a large current flows into one of the bit lines through the Schottky diode, which simultaneously turns on the OFF transistor and increases the collector load current of the previously ON transistor, forcing it to turn off quickly.

Figure 17c illustrates an emitter coupled (ECL) flip-flop which is the basic cell in Advanced Memory System's 64-bit RAM. A specific cell is addressed by raising its word line. The read or write operation is similar to that of the multiemitter cell of Figure 17a, except that the voltage across the selected cell is higher than that across the unselected cell. Thus, a large sense current is available from the selected cell. An advantage of ECL is that an unselected flip-flop has low supply voltage thus requiring low standby power. The cell size and power dissipation of bipolar memories is depicted in Figures 18 and 19.

2. MOS Memories

Since the MOS process contains fewer steps and has a much higher component density than the Bipolar process, it yields a lower cost/ bit semiconductor storage. There are two basic types of MOS memory cells. They are

(1) Static MOS

(2) Dynamic MOS (or charge-storage MOS)

The basic difference between the static MOS cells and dynamic MOS cells is that the former is strictly a bistable device whereas the latter makes use of the low leakage currents of the FET's gate and junctions. These leakage currents are small enough so that the parasitic capacitances have a time constant of the order of a hundred milliseconds or more. The charge on the parasitic capacitance is used for storing memory information.

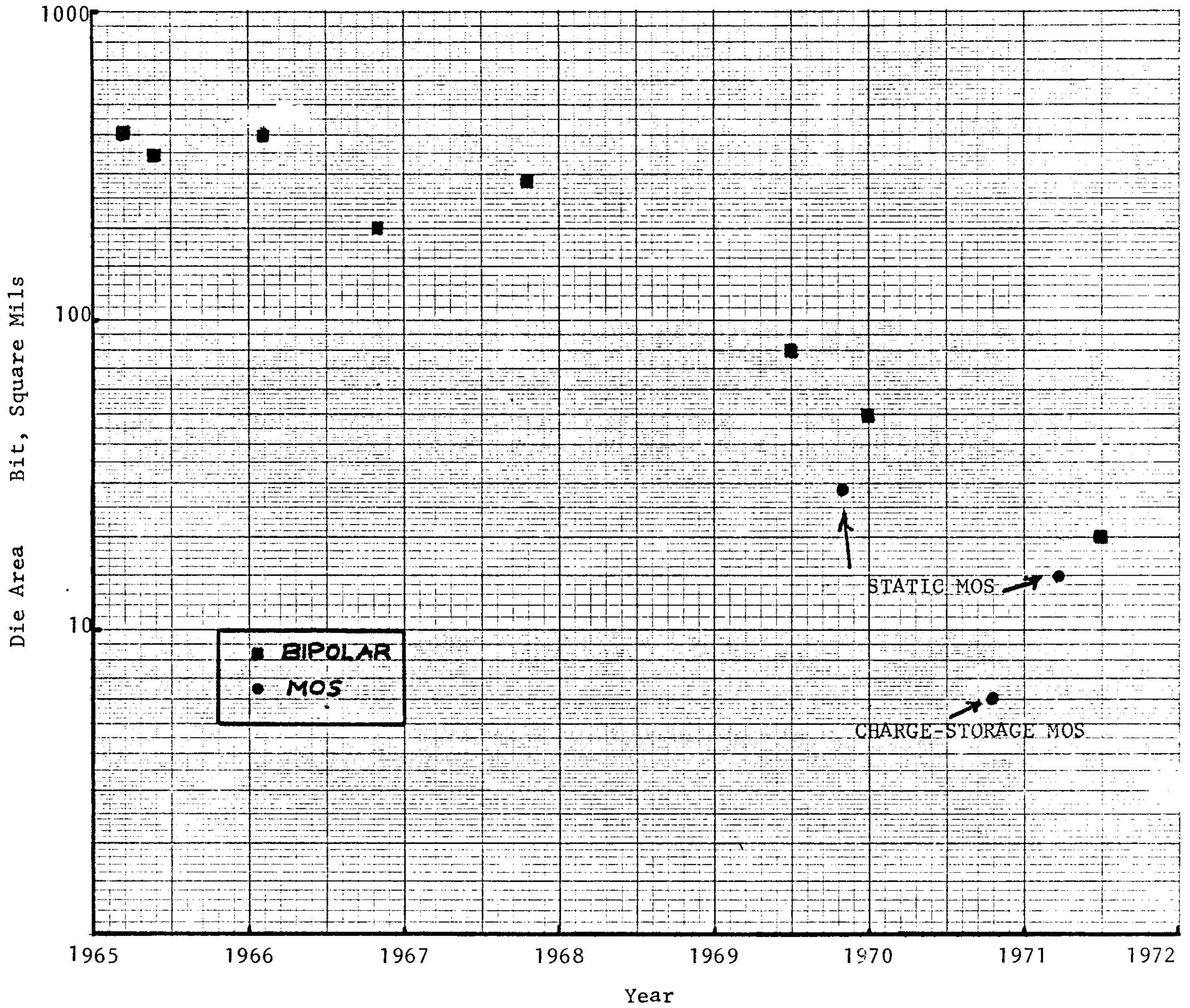


Fig. 18. Cell Size of Bipolar Memory Components as a Function of Time. Static and Dynamic MOS Cells are Included for Comparison.

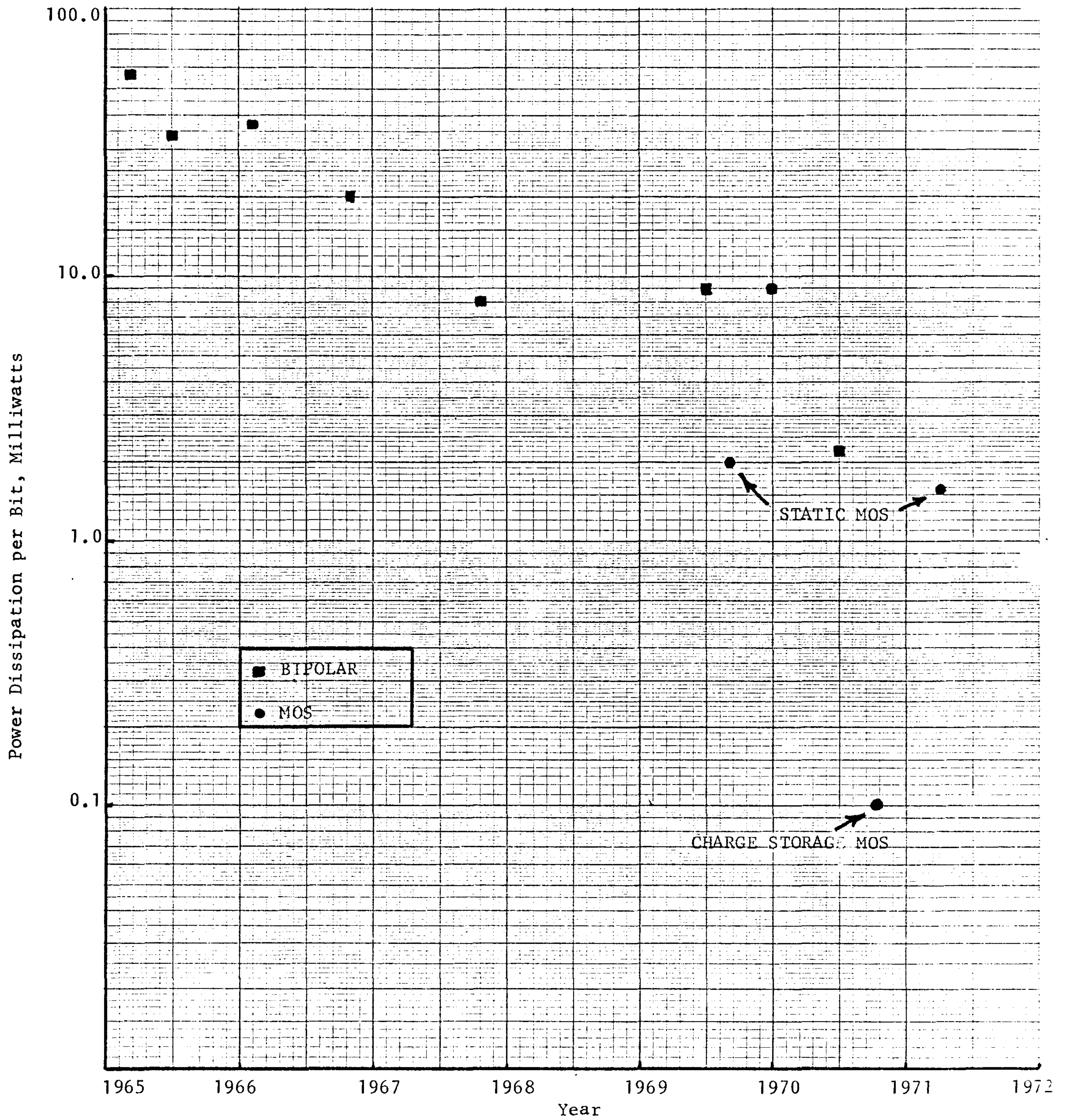


Fig. 19. Power Dissipation of Bipolar Memory Components as a Function of Time. Static and Dynamic MOS are Included for Comparison.

Figure 20 shows the static and dynamic MOS cells. Transistors Q_5 and Q_6 in Figure 20a gate the flip-flop formed by Q_1,Q_2,Q_3 and Q_4. The word line turns on Q_5 and Q_6, transferring the data to the bit-lines for a read operation, and forcing the cell to a logic state determined by the voltage on the bit lines when writing. A common V_{DD} and V_{GG} supply reduces the cell size. However, a lower V_{GG} allows a lower standby power* This circuit is used in most of the 256-bit decoded MOS RAM's manufactured by Intel, Intersil and Computer Microtechnology. Figure 20b illustrates the three transistor dynamic MOS cell used by Intel in their 1k to 4k MOS-RAM. The gate capacitance of transistor Q_1 acts as the charge-storage memory element. Transistor Q_2 connects Q_1 to the read bus when activated by a read enable pulse, while Q provides a write path when activated by the write-enable signal.

3. Comparison of Bipolar and MOS Memories

The major disadvantages of using a bistable cell for storage are:

(1) they dissipate too much power which limits the packaging density.

(2) they occupy too much silicon area which limits the number of bits that can be put on a monolithic circuit.

As against this a Dynamic MOS cell dissipates much less power. Figure 19 shows that a Dynamic MOS cell dissipates at least an order of magnitude less power than the Static MOS cell. However, the charge on the gate capacitance of a Dynamic MOS cell will leak off and therefore periodic refreshing of the charge stored in the cell is necessary. This makes the Dynamic MOS cell slower than Static MOS cell.

Recent announcements indicate that a 4096 bit dynamic MOS RAM array on a 137 mil x 167 mil chip will be available in the near future. This memory chip will have an access time of 300 nsec. and a cycle time of 400 nsec. Active power dissipation is 100uw/bit and the standby power requirement is only 1 uw/bit. The cell size is 2 mil^2 /bit. This is an order of magnitude smaller than the 20 mil^2/bit for Bipolar devices. Efficient realization of n-channel silicon gate technology has made it possible to achieve the smaller cell size, lower threshold voltage and power consumption. Figure 19 gives the power dissipation for typical Static and Dynamic MOS devices.

C. CLASSIFICATION OF SEMICONDUCTOR MEMORIES ACCORDING TO FUNCTION

Semiconductor memories can be classified according to their function as follows:

(1) Random Access Memory (RAM)

(2) Read Only Memory (ROM)

(3) Programmable Read Only Memory (PROM)

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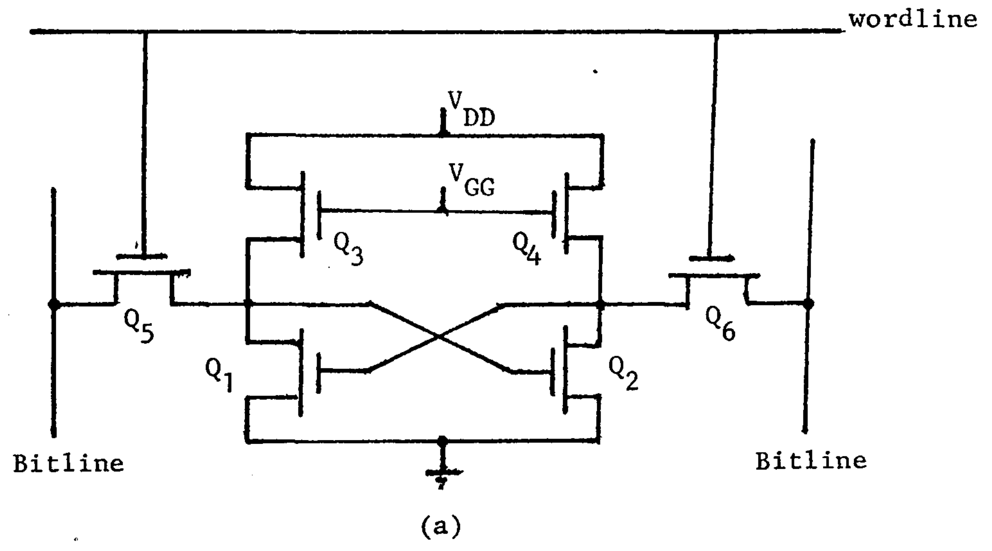
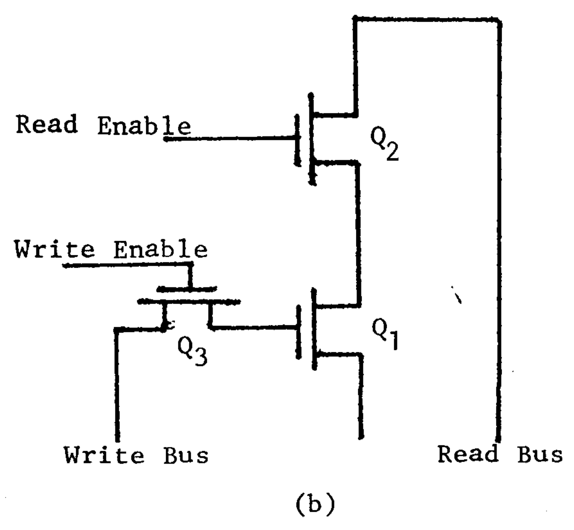
*Standby power is the power necessary to retain the information in the memory cells when no read/write operations are being performed.



(a)



(b)

Fig. 20. (a) Static MOS flip-flop
(b) Dynamic MOS Charge Storage Memory Cell

Company Year	Type of Memory	Type of Technology	Memory Size	Access Time ns	Cycle Time ns	Power Dissipation Active	 Passive
INTEL 1972	RAM	Dynamic MOS	1024 x 1	300	480	240 uw/b	6 μw/b
INTEL 1972	RAM	Bipolar TTL Schottky	16 x 4	35		8 mw/bit	
INTEL 1972	Dynamic Shift Register	MOS	1024 x 1 512 x 2 256 x 4	1-5 MHZ		.1 mw/bit	
INTEL 1971	RAM	Bipolar	256 x 4	60		.5 mw/bit	
MOTOROLA 1972	RAM	Bipolar ECL	64 x 1	10			
NATIONAL SEMICONDUCTOR	RAM	Dynamic MOS	1024	300	480 (read) 580 (write)	250 mw	
NATIONAL SEMICONDUCTOR	RAM	Bipolar	256 x 1				
NATIONAL SEMICONDUCTOR	ROM	Bipolar	256 x 4	36			
NATIONAL SEMICONDUCTOR	ROM	MOS	512 x 8 1024 x 4	1000			
NATIONAL SEMICONDUCTOR	Dynamic Shift Shift	MOS	256 x 4 512 x 2 1024 x 1	200		.1 mw/b at 1 MHZ	
FAIRCHILD	RAM	MOS	512 x 1	400	1000	0.3 mw/b	30 μw/b
FAIRCHILD	ROM	MOS	512 x 8	500			
FAIRCHILD	Dynamic Shift Register	MOS	512 x 1	1-4 MHZ		0.5 mw/b at 2 MHZ	
TI	ROM	Bipolar	256	35		1 mw/b	
HONEYWELL 1971	RAM	MOS	2048 x 1	360	615	75 μw/b	

Table 5. Characteristics of Some Currently Available Semiconductor Memory Chips.

(4) Content Addressable Memory (CAM) or Associative Memory

Table 5 gives specifications of some existing memories.

1. RAM's

RAM's are the most commonly used memories today. Random access means that they can read and write into any arbitrary memory location. The chip area taken by each cell is considerable and hence a single memory larger than 256 bits (Bipolar) has not been produced.

2. ROM's

Semiconductor ROM's are presently more popular than RAM's due to two reasons. The first is the higher density of ROM's and the second is the interest in microprogramming. Once a ROM is built its contents cannot be changed and in that sense it is restrictive. It has another disadvantage in that it has to be custom made. This means that a manufacturer cannot enjoy the economies of large volume production. Therefore RAM's will eventually cost less than ROM's.

3. PROM's

PROM's employ custom made bit-patterns. Mask programmable ROM's use a uniform process with a final mask design for specific customer requirements. Field-PROM's, however, are made by the manufacturer with either all 1's or all 0's and the user programs the array of interconnection either by mechanical scratching or electrical fusing. Sylvania has a 256-bit (32 x 8) scratch-the-surface-type PROM with all logic '0' 's. Current Bipolar PROM's supplied by Harris (64 x 8 bit), Motorola (66 x 8 bit), Signetics (32 x 8 bit), and Monolithic Memories (512 x 4 bit), have a solid nichrome link in each position, located between the address selection line and the output-buffer. The speed of PROM's of this type is about 50 ns. Recent structures use high breakdown currents to cause local melting which destroys the junction. The array cannot be reprogrammed since all the above mentioned changes are irreversible.

Another category of electrically alterable PROM's, on the other hand, can be reprogrammed by a change in the device characteristics. These are known as Read-Mostly Memories (RMM). A 2048 bit (256 x 8) PROM announced by Intel uses a floating MOS gate. Charge can be transferred to the gate by avalanche injection into the oxide from the silicon. Short wavelengths like X-rays or ultraviolet rays can be used to erase the program. This feature allows the memory chip to be completely tested and erased by the manufacturer. Another approach utilizes a semiconducting glass in combination with a silicon structure. The glass has two stable states, one with a conductivity much greater than the other. The glass is switched from one state to another by applying appropriate electrical pulses. However, the glass can be reprogrammed only a finite number of times. This type of PROM's can be read at speeds comparable to Bipolar ROM's. To date, arrays with 256 cells have been made and specified for 200 write cycles.

4. CAM's

CAM's are just now becoming popular and their applications are not completely known. One use of CAM's is as cache memories. It is felt that these memories may have applications in emulation of existing systems. They can also be used to perform a certain class of logic functions.

D. APPLICATION CONSIDERATIONS FOR SEMICONDUCTOR MEMORIES

The choice of memory type would in general depend on cost, performance, nature of applications, power requirements and compatibility with the rest of the system. Where high speed performance is critical, as in buffer memories, Bipolar memories would almost always be used. For small systems Bipolar memories would be cost effective due to lower cost of interface electronics than magnetic core memories. Semiconductor memories are not expected to be used for general minicomputers in the near future due to high cost of the memory power supply. In larger memories (4 to 8k bytes or more) dynamic MOS memories provide the most economical approach.

The two most important disadvantages of semiconductor RAM's are their volatility and power consumption. Volatility does not seem to be a serious disadvanage as computer system designers almost invariably reload a memory after an uncontrolled power down. However, in process control computers non-volatility is important and core memories currently seem to be the best bet. Table 6 (Eimbinder, 1971) depicts a comparison of semiconductor and magnetic characteristics for a megabit memory.

One other consideration in the application of semiconductor memories is the number of bits that can be outputted in parallel. One of the major restrictions on the number of bits that can be outputted is the number of pins on the package used. Figure 21 shows a graph of the number of pins required for different organizations of a 4096 bit memory. (It is assumed that two pins are required for power.) The graph shows that the number of pins grows very rapidly as the number of parallel output bits increase. Since the number of accesses to the memory will depend on the number of bits required to make up a word, the organization of the memory should be kept in mind. The next section will discuss some existing organizations of memory elements on a chip and the considerations in making memory systems using these chips.

E. MEMORY CHIP ORGANIZATIONS AND MEMORY SYSTEMS

A memory system consists of two distinct parts - the memory array (i.e., array of storage locations) and a set of support circuitry. LSI memory chips are currently manufactured to contain a memory array and some subset of the requisite support circuity. The memory array can be organized as an M x N array with M words N-bit in length, i.e., a 256 bit memory can be organized as a 256 word x 1 bit, 128 word x 2 bit, 64 word x 4 bit, etc. module. The support circuitry includes the memory address register and decoder, sense and write amplifiers, row and column drivers, etc. Typical delay times through sense/write amplifiers is 35 ns. Decoders can introduce

	Readout	COS MOS (NDRO)*	Bipolar (NDRO)	Core (DRO)**	Plated Wire (NDRO/DRO)	Thin-Film (DRO/NDRO)
Unit Cell	Read delay (ns)	10	5	150	20	10
	Write delay (ns)	25	5	150	20	10
	Standby power (μW)	10	1000	0	0	0
Array of cells	Array size, bits	256 x 1	128 x 1	16k x 18	4k x 128	1024 x 64
	Word select I (mA)	1	20	425	900	200
	Digit write I (mA)	1	20	425	20	15
	Drive voltages (V)	5-15	2	30	20	10
	Readout signal	200 μA Dc	500 μA Dc	20-mV Pulse	10-mV Pulse	2-mV Pulse
	Packing density (bpsi)	15k	7.2k	4.5k	1450	3200
	Rise time of read current (ns)	-	-	100	30	10-35
	Curie temp. (C)	-	-	500-600	600	600
	Volatility	Yes	Yes	No	No	No
10^6 Bit Memory	Economic module, bits	2-32k	1-8k	256k	256k	64k
	Power dissipation (W)	50	1000	100	200	200
	Full cycle time (ns)	125	50-100	500	200	200
	Cost per bit (cents) in mass production	2-5	4-5	1-2	2-4	2-3
	Mode of organization	LS***	LS	2-1/2D	LS	LS
	Batch fabrication	Yes	Yes	No	Semi	Yes

*NDRO = Non-Destructive Read Out

**DRO = Destructive Read Out

***LS = Linear Select

Table 6. Comparison of Semiconductor and Magnetic Characteristics for a Megabit Memory [Courtesy, Eimbinder 1971]

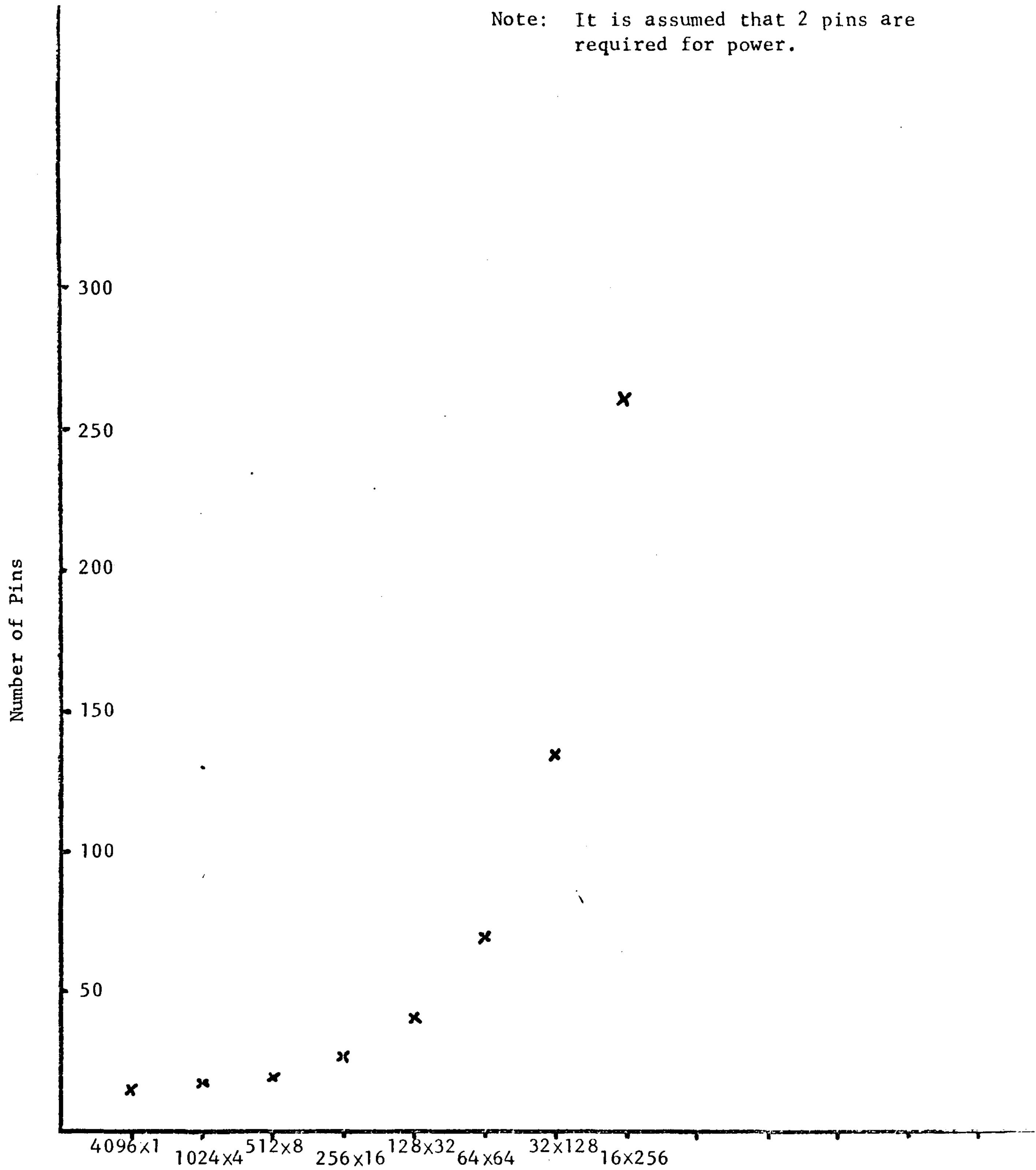


Fig. 21. A Graph of Number of Pin Requirements for Different Memory Organizations of 4K bits.

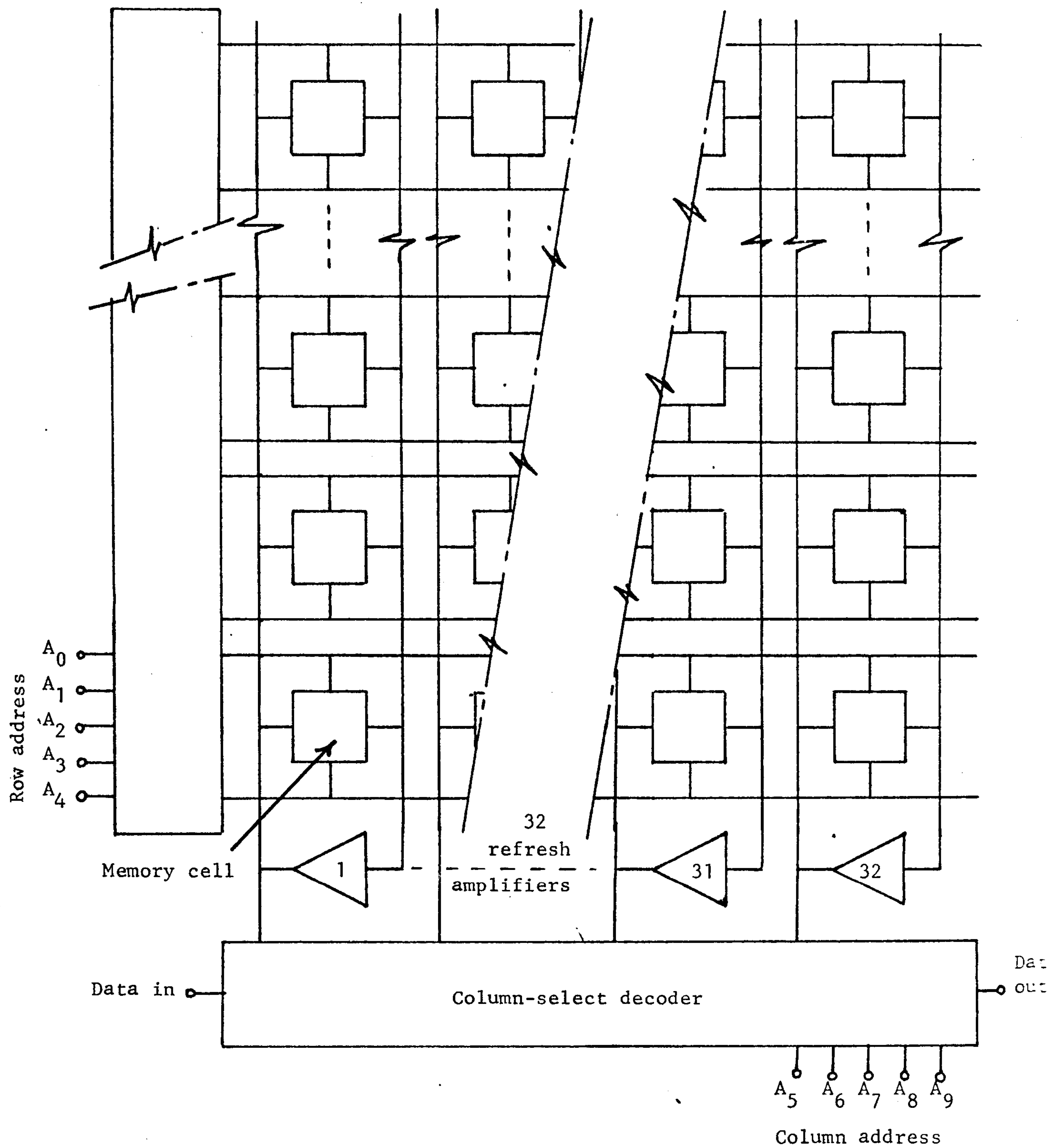
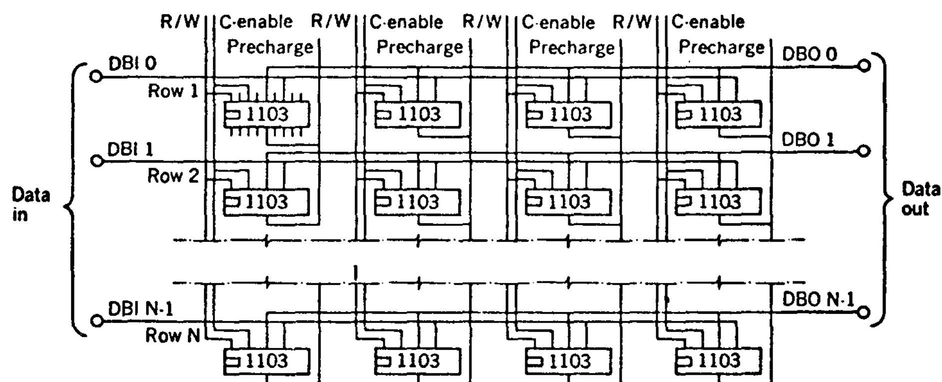
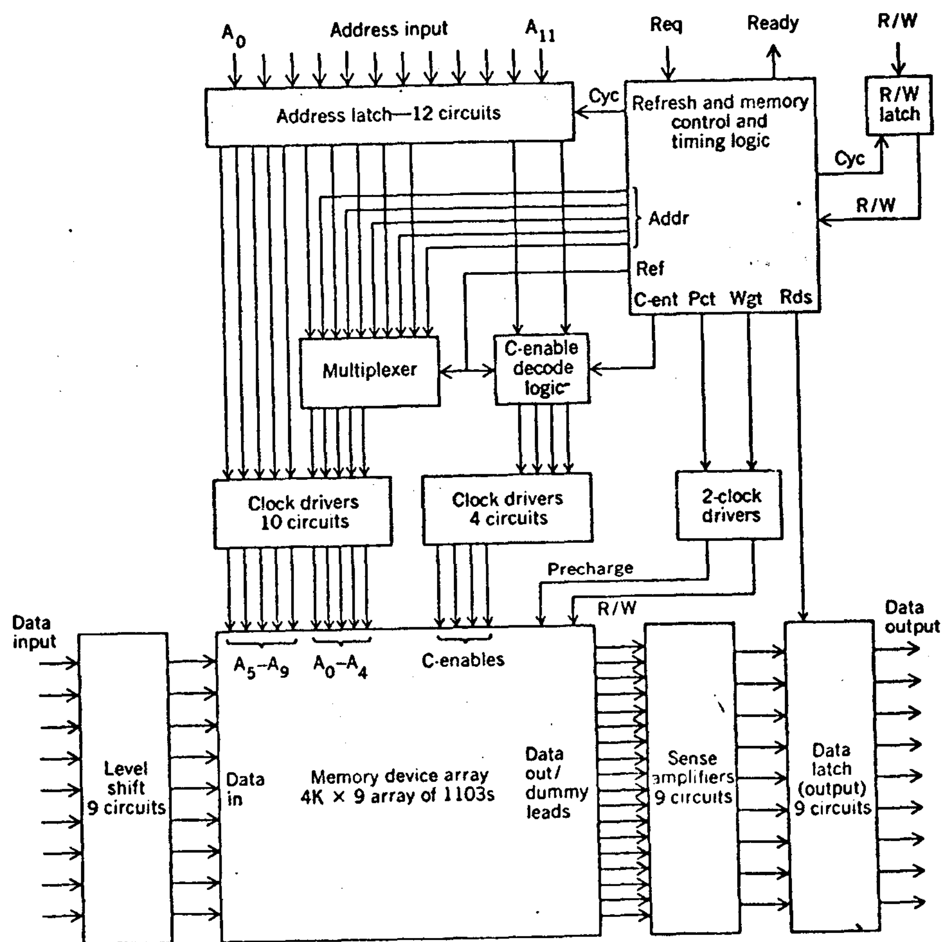


Fig. 22. Organization of a Fully Decoded 1024-bit Charge-Storage MOS Memory Chip.



(a)



(b)

Fig. 23. Organization of a memory system that uses fully decoded 1024-bit memory components. The memory component, marked 1103, can be connected in an array of 1024M words by N bits. System access times of under 250 ns and cycle times of under 400 ns are achievable with such memories. (a) - Organization of the memory plane. (b) - Block diagram of a 4096-word by 9-bit memory system.

additional delays of about 10 ns. An important consideration in selecting a memory chip is the amount of support circuitry integrated on the chip. The use of external support chips results in additional cost and propagation delays. If the above mentioned circuits are included inside the memory chip, the delay times are lower due to shorter distances and absence of external capacitances.

Figure 22 (taken from Vadasz et al. 1971) depicts the basic organization of Intel's 1103, a fully decoded 1024-by-1 dynamic RAM, which uses the memory cell shown in Figure 20b. Figure 23 (taken from Vadasz et al. 1971) shows how the memory components (1103) can be connected in an array of 1024 M words by N bits. Note that the address and clock inputs require a level shifter that converts a TTL level to the higher voltage level required to drive the dynamic MOS array. Additional circuitry for periodic refreshing of information in the cells is also shown. Intel's latest fully decoded 4096-bit dynamic MOS RAM accepts TTL compatible inputs.

F. FUTURE OF SEMICONDUCTOR MEMORIES

The computer industry does not report sales volume in a formal way, so it is difficult to get accurate figures. The present growth rate indicates that the computer market doubles every two and one half years (Electronic Products Jan. 1970). The sale of semiconductor memories is increasing day by day. The first ROM available was small (256 bits) and slow (2 usec. access time). But today MOS ROM's can be purchased in configurations providing speeds up to 750 nsec. with capacities as large as 4096 bits and cost that cannot be approached by any other technology. The appropriate costs of a 4096 bit MOS ROM in 1970 and 1975 are shown in Figure 24. It is expected that by 1975 single semiconductor memories as large as 16K bits would be available.

It is expected that semiconductor memories will eventually replace the secondary storage devices such as drums and discs. It is predicted that one-third to one-half of drum and disc business will be taken up by semiconductor memory in the late seventies. [Graham, Hoff 1970] An eight megabyte MOS shift register configuration priced at less than one cent/bit was recently advanced as competition to drums. It operates at a 1 Megacycle clock-rate with 20 to 50 times the drum access rates. Its advocates claim that the arrangement is two times as efficient as a drum in terms of system bit utilization, hence making it comparable to today's drum costs [IEEE Computer Jan/Feb 71].

Bubble memories, thin film and plated wire memories are other competitors for secondary storage. Thin films would be replaced by Bipolar memories where speed is required and by plated wire where radiation resistance and volatility are the predominant considerations. By 1980 semiconductor memories are expected to account for two-thirds of the market.

Figure 24 is a prediction of high volume selling prices for various technologies. There are many claims made by each manufacturer regarding their product and the cheap price at which they will be able to sell. Only the future will verify which claims are true.

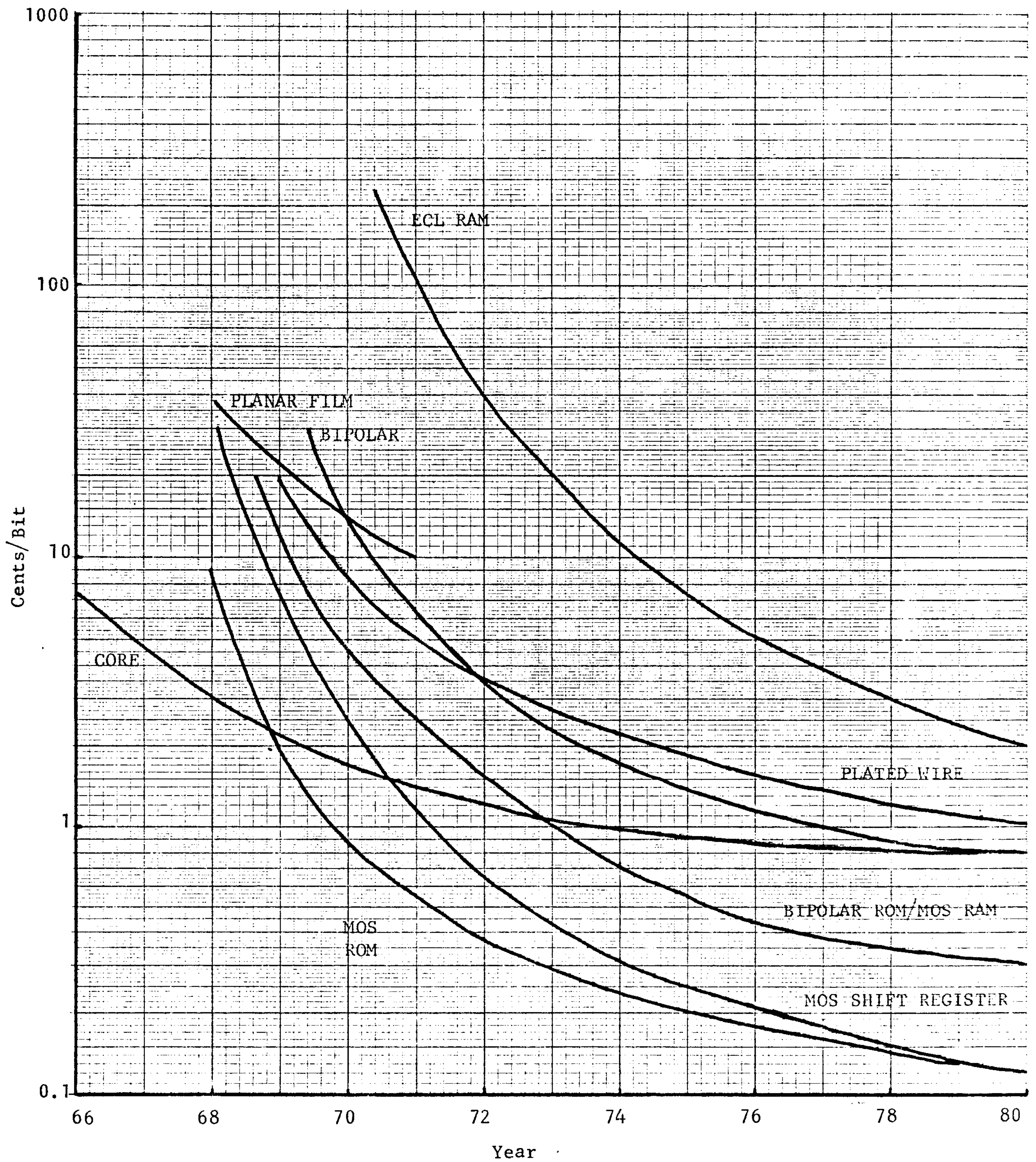


Fig. 24. High Volume Price Forecast for Semiconductor Memories.

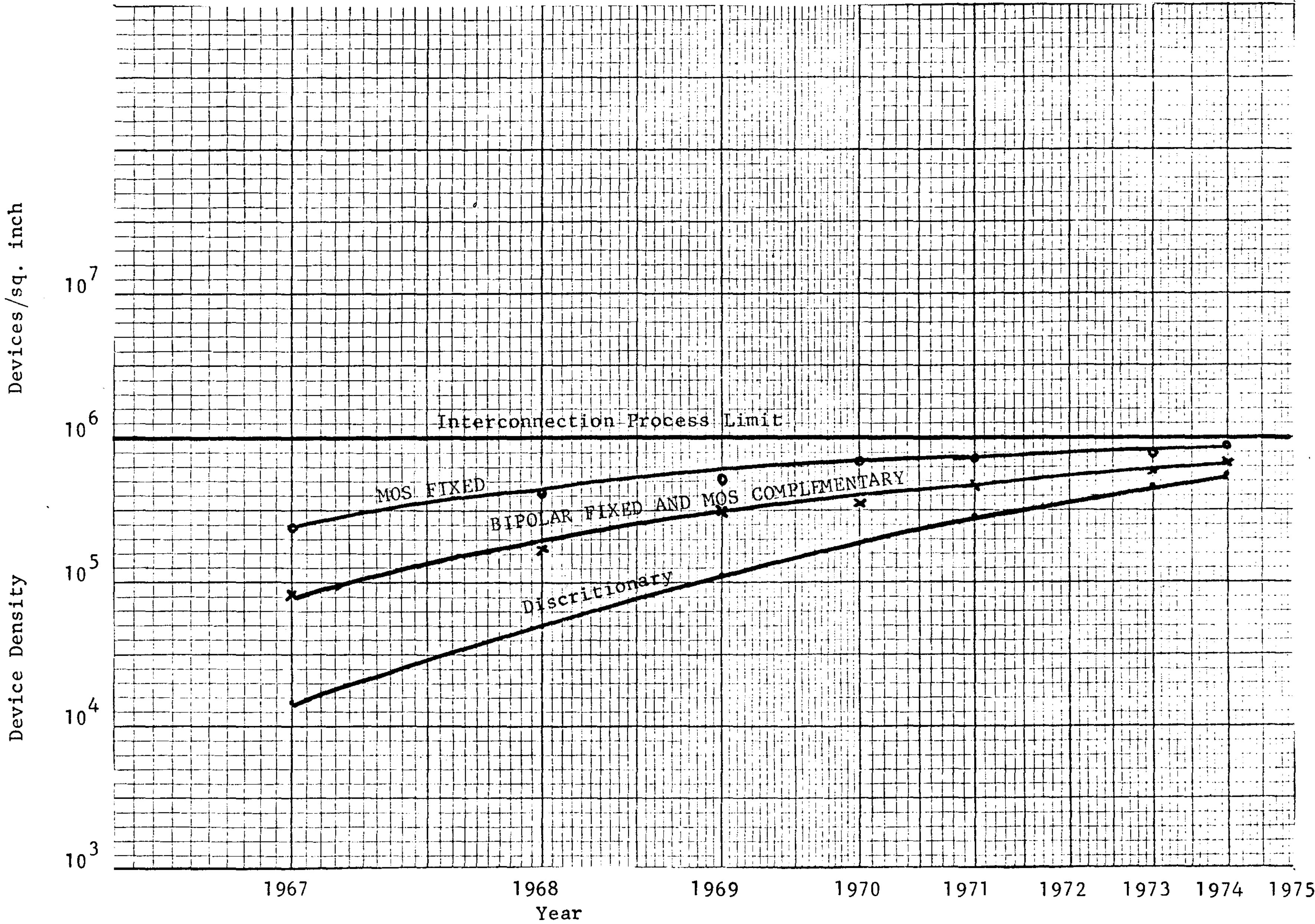


Fig. 25. Ten Year Forecast of Device Density.

VII. LSI AND LARGE MODULES

Large Modules and Large Scale Integration go hand in hand. Large Modules are a direct consequence of Large Scale Integration and certain other considerations such as higher level (Register Transfer level) design.

LSI has a large impact on the logic in a digital system.

1. It has brought down the price of a logic device by several orders of magnitude from the days of vacuum tubes and transistors.

2. It has increased the overall speed of the logic circuit by putting many circuits on the same chip thus reducing the delays in signal transmission.

3. It has reduced the size of the overall system due to high device density.

4. It has decreased the cost of the overall system due to decreasing the number of interconnection requirements.

5. It has increased the reliability of the overall system by an order of magnitude and

6. The application range of logic devices has widened such as digital wrist watches of the future.

LSI technology and its predicted trends yields us certain insight into what restrictions one should keep in mind and what would be the right method of designing Large Modules in an optimal way.

A. SIZE OF THE LARGE MODULES

The size of the Large Modules that is essentially the number of devices on each module, should be chosen carefully. A ten year forecast of device density for various logic is shown in Figure 25. A forecast of 3" diameter silicon slice by 1976 has been made (Petritz, 1966). Assuming a device density of 10^6 devices/sq. in. by 1976 this gives a total device count per chip of 7.05 x 10^6 devices. Giving a safety factor of about 10 one can easily assume a single chip with 7 x 10^5 devices on it. This means that Large Modules could be fabricated on single chips if their device count is within this limit.

B. PIN LIMITATIONS ON LARGE MODULES

The present packaging technology shows that there is going to be a severe pin limitation on Large Modules. Even though packages with 300 pins are forecasted it does not seem possible that they would attain the economies of batch fabrication in the near future. EDN staff (1970) comment that "The commercial side of the business has a standard in the DIP and is not in any hurry to change. Its interest in LSI

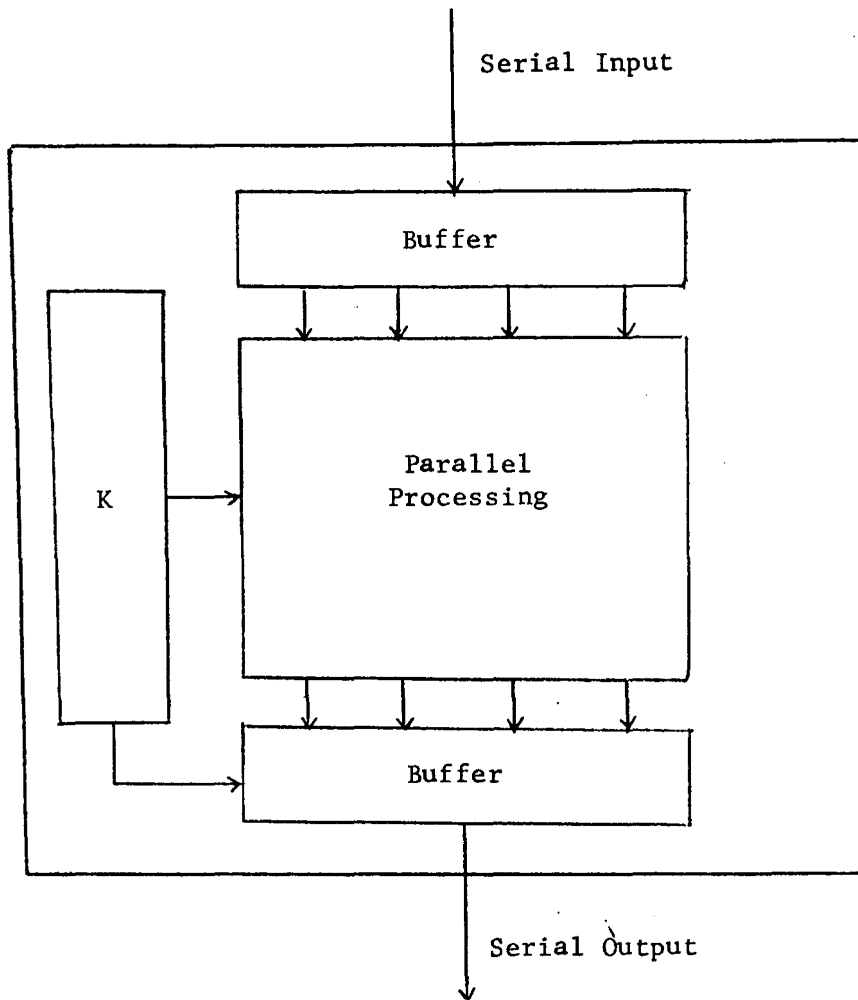


Fig. 26. A conceptual design of a Large Module showing serial input and output to conserve pins.

includes a DIP with 40 pins." Therefore 40 to 60 pins per package seems to be optimal. If the data width of the Large Modules is going to be large (say 64 bits) then, for the sake of speed, it may be necessary to process the data in parallel internal to the chip with serial intercommunication between chips . Figure 26 shows such a configuration. This should not be much of a restraint as the available amount of Logic internal to a chip is large. Thus the design of Large Modules should have a goal of high density with low pin counts.

C. LOGIC DESIGN OF THE CIRCUIT

For LSI fabrication it is essential that the logic be regular, i.e., an array of logic rather than random logic. LSI Computer Systems, a manufacturer of custom-designed MOS chips, has announced a 200 sq. mil chip with an equivalent of 1200 TTL gates if the logic is random. As against this, the same chip can have 12,000 TTL equivalent gates if the logic is regular. The propagation delay for the random logic chip is of the order of 40 nsec/gate as against 20 nsec/gate in the case of the non-random logic chip. These figures indicate that the logic design should be done in an array fashion to accomplish maximum advantage of LSI. This means that one should not map the existing logic directly on to the chip, i.e., a module designed for MSI chips should not be mapped into an LSI chip but should be redesigned to give more optimum results.

D. PARTITIONING OF THE LOGIC

Logic partitioning is a very important consideration. The amount of logic on a chip is not as serious a problem as the number of available pins. At times the same circuit may be repeated on two chips if this results in fewer I/O pin requirements.

E. MEMORIES FOR LARGE MODULES

Semiconductor memories are becoming more popular and they should be used in these modules. There is a choice as to the type of memory. RAM's and PROM's seem to be the best bet as they will be produced in volume. CAM's may be applicable sometimes as cache or buffer memories. It may also be possible to put some logic inside the memory. Instructions like moving contents of a cell from one location to another location or adding two locations and storing in a third location could be done inside the chip itself. Knuth's analysis of Fortran program shows that these kinds of instructions form the major percentage of instructions in Fortran programs.

F. THE CONTROL PART OF LARGE MODULES

A repetitive structure is best for the control part of Large Modules. This implies that microprogramming using RAM or ROM structures would be the right solution. The former have the advantage that they will be less costly and can be dynamically changed whereas the latter are faster and non-volatile.

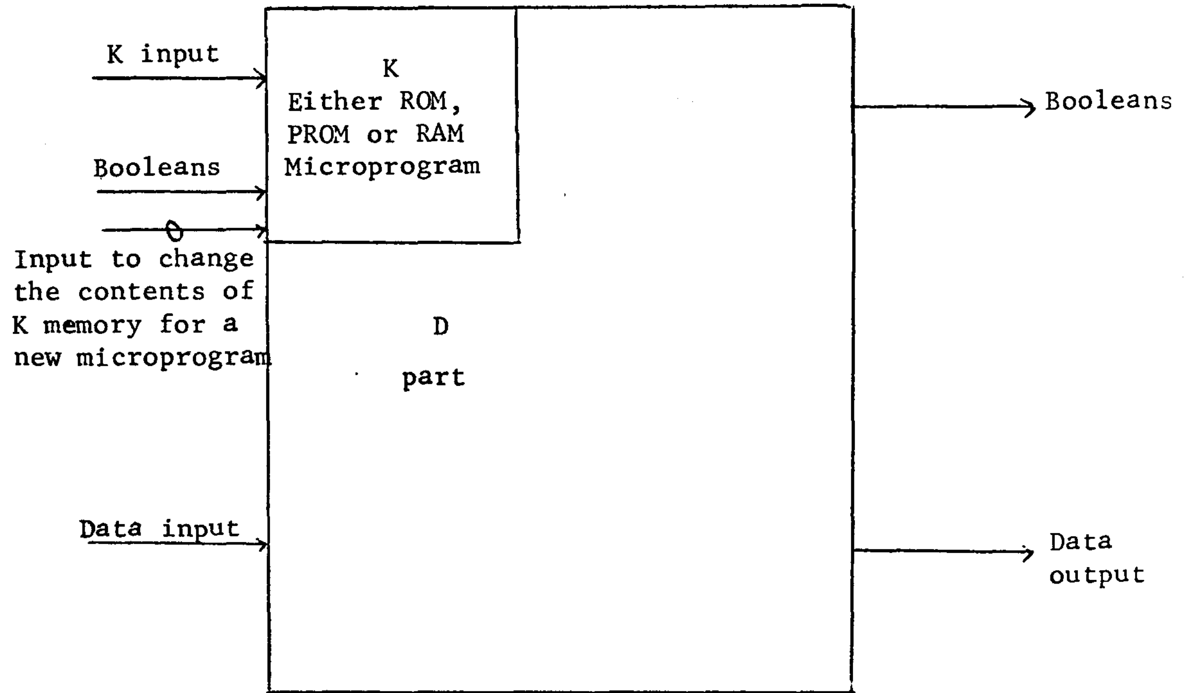


Fig. 27. A Large Module with Microprogrammed Memory.

The idea of using RAM or ROM for modules lends itself to a very interesting consequence. By changing the ROM on the module or the microprogram in the RAM and keeping the data part of the module the same, conceivably different functions could be achieved from the same module. Figure 27 shows such a structure.

G. CHANGE IN THE DESIGN OF LARGE MODULES

In LSI the development costs are exorbitant. It is very essential that the initial design be checked out completely before the fabrication is done. A single change in the circuit would mean a loss of ten (or more) thousands of dollars.

In designing modules all the above goals do not seem very difficult to achieve and the promise for Large Modules seems to be very encouraging from a technology point of view.

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